Usage of SKiiP Systems (SEMIKRON integrated intelligent Power)

1 Main Features of SKiiP Systems

- SKiiP: SEMIKRON Intelligent Integrated Power is a power semiconductor subsystem
- SKiiP integrates power semiconductor switches, heat sink and gate driver unit with protection and monitoring circuit
- SKiiP3 is the successor product for SKiiP2 with increased power density and is compatible to SKiiP2
- based on SKiiP pressure contact technology which allows a compact power module design with very low thermal resistances, high thermal cycling capability and low parasitic stray inductances.
- equipped with closed loop current sensors, used for short circuit and over-current protection
- Normalized analog voltage signals of the actual AC-current value, the actual ceramic substrate temperature value and the actual DC-link voltage value (optional, depends on type) are available at the DIN41651 gate driver connector of the SKiiP for use in the control unit.
- Assembly of SKiiP is based on SKiiP technology, a pressure contact technology which allows a compact power module design with very low thermal resistances and high thermal cycling capability.

2 Type Designation System

	SKiiP	❶	❷	❸	❹	❺❺	❻❻	❼		❽❾❾		❿	
SKiiP2 example *:	SKiiP	3	4	2	G	D	1	2	0	- 3	DU		L
SKiiP3 example:	SKiiP	5	1	3	G	D	1	2	2	- 3	DU		L

❶ nominal current I_C (@ $T_{heat\ sink}$=25°C) divided by 100 as e.g. 500A → 5, can contain 2 letters eg. 15,

❷ SKiiP2: chip specification / SKiiP3: insulation DCB (direct copper bonded) ceramic substrate type
0→ standard aluminum nitride (AlN) DCB ceramic (SKiiP3 only)
1→ standard aluminum oxide (Al_2O_3) DCB ceramic
❸ SKiiP generation , e.g. 3 for 3rd generation
❹ chip type as e.g. G = IGBT
❺ circuit
B → 2 pack (half bridge, dual)
H → 4 pack (single phase bridge)
D → 6 pack (3 phase bridge)
DL → 6 pack + brake chopper
❻ voltage class
06 → V_{CES} = 600 V
12 → V_{CES} = 1200 V
17 → V_{CES} = 1700 V
❼ chip generation
❽ number of used modular half bridges (2 packs)
❾ gate driver designator
DU → gate driver with DC-link voltage measurement and over voltage protection
D → gate driver without DC-link voltage measurement
DUF → gate driver with DC-link voltage measurement, over voltage protection and F-Option (optional for GB type only)
DF → gate driver without DC-link voltage measurement and F-Option (optional for GB type only)
❿ heat sink designator
L → standard profile for forced air cooling
W → standard profile for liquid cooling

*** Please note:** Information about the former SKiiP2 standard types before 01/04 (e.g .about type designation) is available on request.

3 Which SKiiP System should I use?

Generally speaking SKiiP3 is recommended for new designs when a suitable type is available, especially in applications where a very high power density is required. The table gives a survey of the available types (n.a. ⇔ not available; I_C given at T_j = 150°C, T_s = 25°C).

	6 pack (GD)	6 pack with brake-chopper (GDL)	2 pack (GB)
SKiiP2	I_C	I_C	I_C
600V	200A - 400A	contact SEMIKRON	800A - 1600A
1200V	150A - 300A	150A - 300A	400A - 1200A
1700V	150A - 250A	contact SEMIKRON	500A -1000A
SKiiP3	I_C	I_C	I_C
600V	400A - 800A	n.a.	n.a.
1200V	300A - 600A	n.a.	1000A - 2400A
1700V	500A	n.a.	1000A - 2400A

Please note for SKiiP3 there do exist two types of ceramic substrate, Aluminum Nitrite and Aluminum Oxide. The first one has a very good thermal conductivity which is suitable in water cooled applications, whereas the later one is basically supposed for standard air cooled applications. For SKiiP2 only Aluminum Oxide is used.

4 Technical Explanations

4.1 SKiiP technology

SKiiP technology is the patented technology on which SKiiP Systems are based. The main characteristic features of SKiiP technology are

- the base plate free power section
- the spring pressure contact of all thermal and electrical contacts
- the internal low inductive paralleling of inverter legs

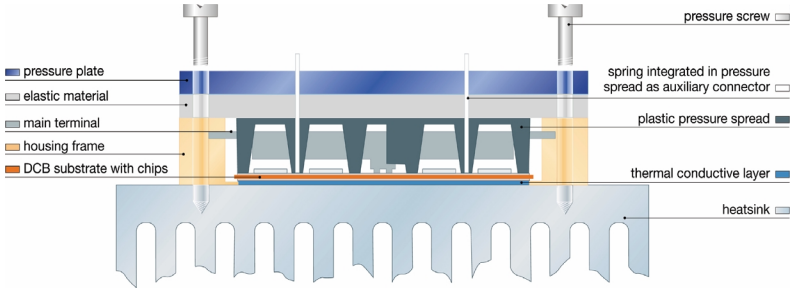


Fig. 1 SKiiP System power section assembly

The electrical main and auxiliary terminals are not soldered to the insulated ceramic substrate but pressed. The insulated ceramic substrate is pressed to the heat sink. The pressure contacts are responsible for superior thermal cycling capability of SKiiP Systems. In addition they provide simple assembly.

Fig. 2 shows the paralleling of ceramic substrates to achieve high output current capability. This feature of the SKiiP technology provides low stray inductance values in the commutation circuit and therefore allows high utilization of the IGBT blocking voltage Vces.

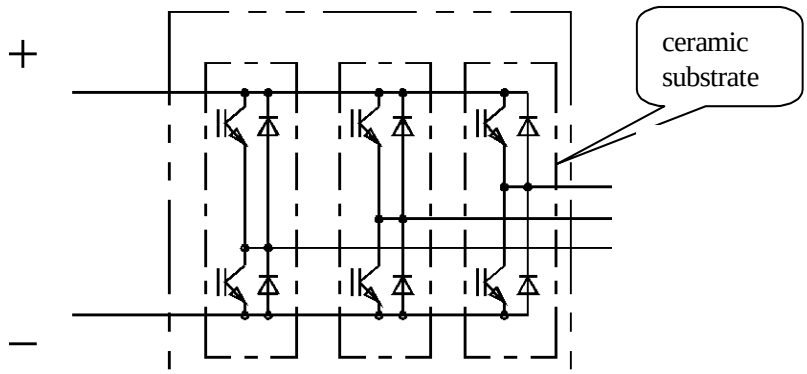


Fig. 2 Paralleling of ceramic substrates

4.2 Family of Standard SKiiP Systems

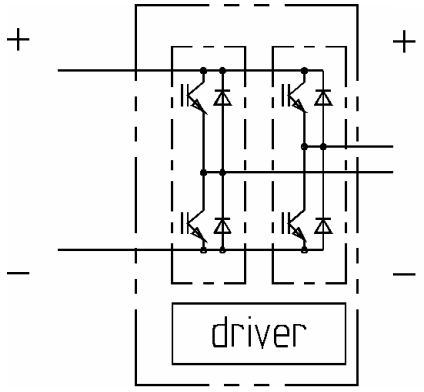


Fig. 3 2-fold SKiiP System

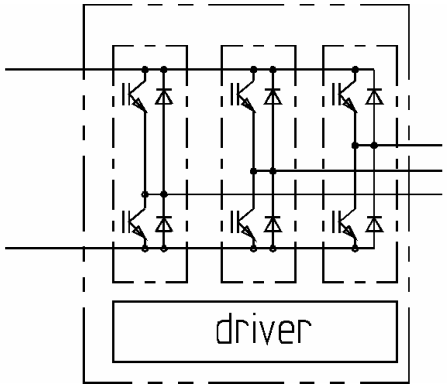


Fig. 4 3-fold SKiiP System

One SKiiP system contains 2, 3 or 4 single ceramic substrates as shown in the block diagrams.

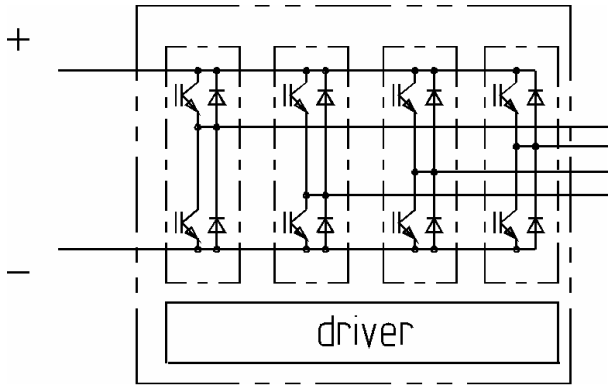


Fig. 5 4-fold SKiiP System

Each ceramic substrate contains a full phase leg with upper (TOP) and lower (BOTTOM) IGBT as well as the corresponding freewheeling diodes. The integrated gate driver defines the circuit. The following table gives a survey of the available circuits:

	2 substrates (2-fold)	3 substrates (3-fold)	4 substrates (4-fold)
circuit			
GB	SKiiP2/3	SKiiP2/3	SKiiP2/3
GD		SKiiP2/3	
GDL			SKiiP2

Please note: To parallel 2, 3 or 4 power sections of the SKiiP System type the user must parallel the DC and AC terminals to each other. SEMIKRON recommends dedicated bus bars for AC terminal paralleling (please refer to chapter "Accessories").

4.3 Insulation

Magnetic transformers are used for insulation between gate driver primary and secondary side. The circuit used for the DC voltage measurement is designed, manufactured and tested according to standard EN50178 (VDE 0160). The temperature sensor is insulated on the ceramic substrate.

Please note: the insulation of the temperature signal is a basic insulation only. Equipment which is designed according to EN50178 must have further insulation for all parts which might be touched by a person.

The SKiiP System insulation test voltage is depending on Vccmax. The individual insulation test voltage level is given in the data sheets.

4.4 Properties of the GB and GD gate driver

4.4.1 User Interface - Digital Inputs

The figure below shows the schematic of the SKiiP 2 and SKiiP3 digital input lines. A 1nF capacitor is connected to the input to obtain high noise immunity. This capacitor can cause for current limited line drivers a little delay of few ns, which can be neglected. We recommend choosing the line drivers according to the demanded length of the ribbon cable.
It is compulsory to use circuits which switch active to +15V and 0V. Pull up and open collector output stages must not be used for TOP/BOT control signals.

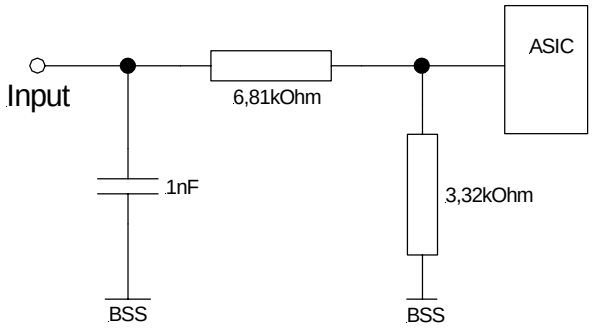


Fig. 6 User Interface - TOP/BOT input

4.4.2 User interface - Analog Outputs

The figure below shows the schematic of the SKiiP2 and SKiiP3 analog output lines. The 475Ω resistor in series with the voltage follower does avoid short circuit damages. Please ensure that the maximum driven current by the output operational amplifier does not exceed 5mA.

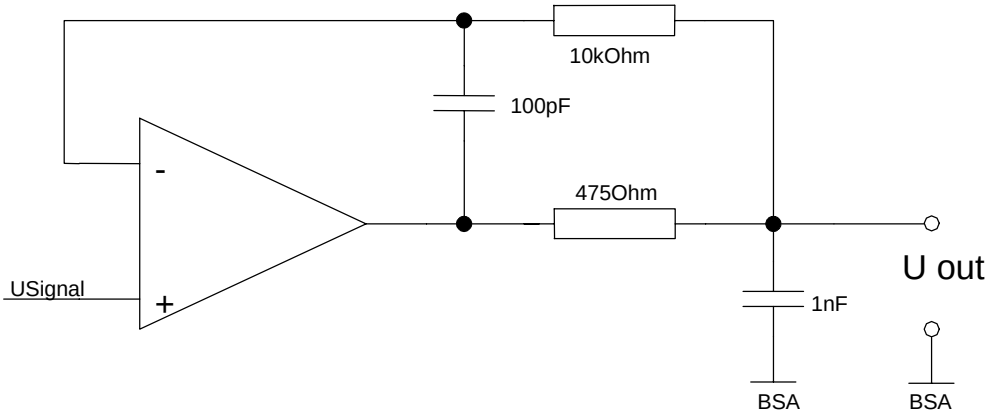


Fig. 7 User Interface- Analog Signal Output

For a trouble-free interaction of SKiiP and user side control it is necessary to adapt the customer input to the SKiiP outputs. For that reason the auxiliary analog signal ground BSA shall be used when analog signals are measured. The ground BSA is on the SKiiP driver board on the same potential as BSS, which is the ground of the power supply. The difference is that the BSA line is not used for supply currents and for that reason no voltage drop due to supply current will be caused.
In the following section a schematic and a description is given for an analog input circuit on the controller board of the user.

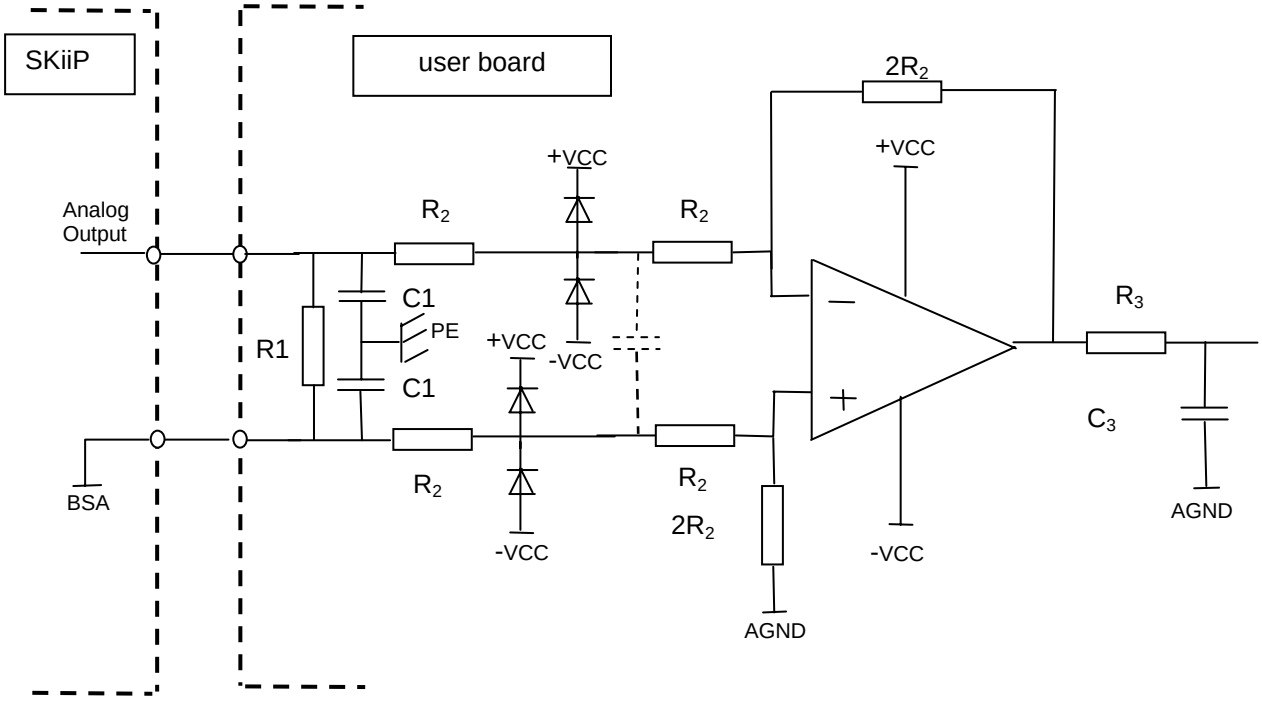


Fig. 8 Symmetric Wired Differential Amplifier

The circuit above is a symmetrical wired differential amplifier.

- At the input is a 10kΩ resistor (R_1). The interference sensitivity of the over all circuit (user control, driver) is reduced by a continuous current flow through this resistor.
- The capacitor C_1 leaks differential and common mode high-frequency interference currents. This capacitor should not be larger than 100pF to ensure that there is no additional time delay in the system.
- The symmetrical wiring of the amplifier is as follows. Please note that no capacitor is in parallel to the feedback resistor and also to the resistor of the non-inverting input to ground ($2R_2$). These

capacitors have often higher tolerances, so the common-mode rejection of the circuitry is reduced by this effect.

- The input resistor should be split up and installed between the clamping-diodes. The current in the diodes is limited by this resistor. A diode with a low reverse current should be selected e.g. 1N4148.
- If a low pass filtering shall be implemented in the input circuit, this should be done with a capacitor between the input resistors (see dotted lines). In most cases this capacitor is not necessary and the smoothing can be realised by a simple R-C network (R_3, C_3) at the end of the operational amplifier.

4.4.3 Requirements of the Auxiliary Power Supply

The table shows the required features of an appropriate power supply for a SKiiP System. In case that the gate driver is supplied with 24V it is possible to use 15V provided at the DIN 41651 connector of the gate driver as an auxiliary power supply, e.g. for a level-shifter at the controller's output signals.

	SKiiP2	**SKiiP3**
unregulated 24V power supply	20V - 30V	13V - 30V
regulated power supply 15V ± 4%	15V	please use input of unregulated 24V power supply
Iout15V (can be used if 24 V supply is active)	< 50 mA	< 50 mA
mimimum peak current of auxiliary 15V supply	1,5A	-
mimimum peak current of auxiliary 24V supply	1,5A	1,5A
max. rise time of auxiliary 15V supply (the voltage slope has to be continuous – no plateau in voltage slope)	50 ms	-
max. rise time of auxiliary 24V supply (the voltage slope has to be continuous – no plateau in voltage slope)	50 ms	< 2 s
power on reset completed after	130 ms	150 ms

Please note: All values are related to one SKiiP. Do not apply switching signals during power on reset.

The current consumption of SKiiP Systems depends on the level of supply voltage used, the standby current of the gate driver, the switching frequency, the capacitance of the IGBT gates in use and on the actual main AC-current. In the data sheets for each gate driver an equation is given which describes the current consumption depending on standby current, switching frequency and AC output current. Please rate the power supply that way, that the continuous current is at least 20% higher that the calculated consumption current from the SKiiP. The rated peak current of the supply must fulfill the specification in the table.

Since SKiiP3 uses a switched amplifier for the compensated current sensor the current consumption of SKiiP3 has been reduced towards SKiiP2.

In the datasheets the equation for the evaluation of the current consumption is given assuming supply with 24V. Additionally the SKiiP2 datasheets provide an equation to calculate supply current for operation with 15V.

Example for SKiiP2:

I_{S2} = supply current @ 24V supply voltage = 340mA (stand by current) + 490mA * f_s/f_{smax} (current depending on switching frequency.) + 3,5mA*I_{AC}/A (current depending on output current I_{AC})

Example for SKiiP 3

I_{S2} = supply current @ 24V supply voltage = 280mA (stand by current) + 460mA * f_s/kHz (current depending on switching frequency.) + 0,0003mA *(I_{AC}/A)^2 (current depending on output current I_{AC})

Please note: The switch mode amplifier of SKiiP3 compensated current sensor causes a quadratic relationship to AC current level.

4.4.4 Gate Driver Block Diagram

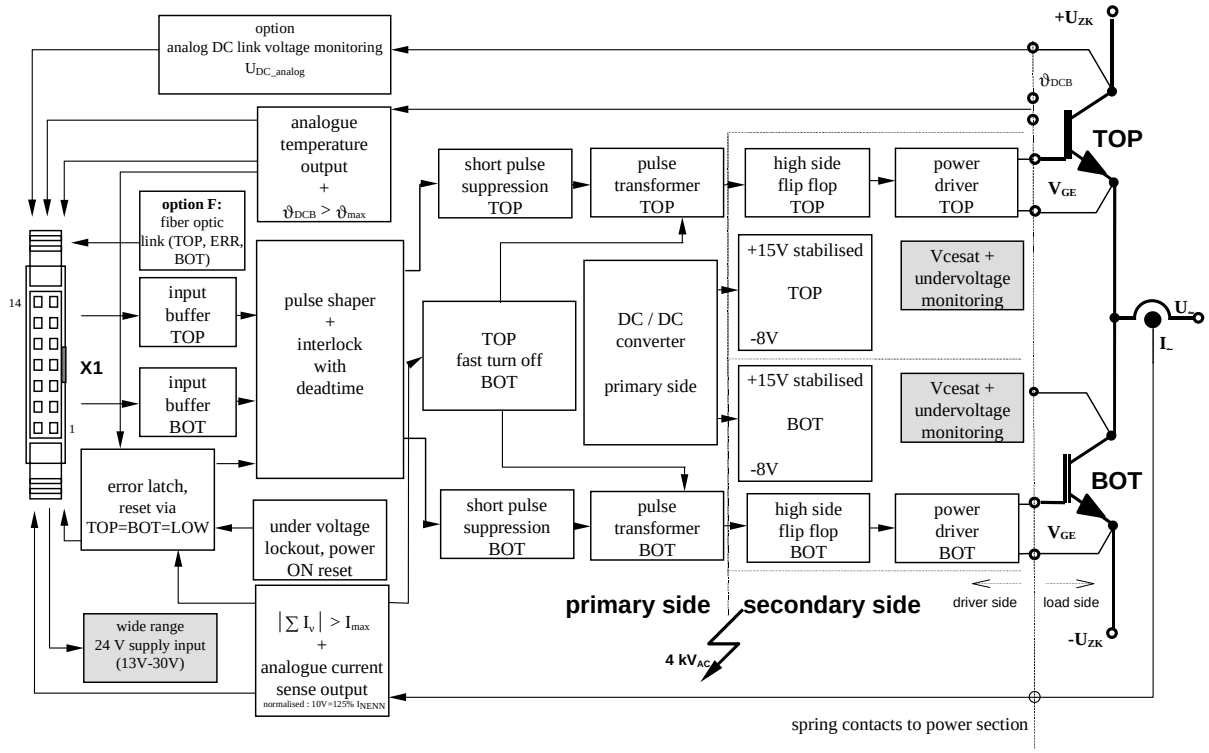


Fig. 9 Gate driver block diagram

Fig. 9 shows the functionality of the phase leg (⇔2-pack) gate driver in a block diagram. The 6 pack gate driver incorporates the same functionality per phase. Additionally SKiiP2 features a ground fault protection. Trip levels of the ground fault protection are given in the corresponding data sheet. The table below shows a list of functional differences between SKiiP2 and SKiiP3 gate driver:

Property	SKiiP 2	SKiiP 3
power supply	20 V - 30 V + 15V regulated	13V - 30V
ground fault protection (GD)	Yes	No

4.4.5 Protection and supervisory functions

SKiiP2/3 gate drivers feature the following protection and supervisory functions

- interlock and dead time generation for TOP and BOTTOM IGBT
- short pulse suppression
- input pulse shaping
- input signal clamping
- under voltage monitoring of the (internal) supply voltage on primary side

- transient over voltage and inverted polarity protection by suppressor diode
- over temperature protection (if forced air cooling is used)
- short circuit and over current protection
- Vcesat protection
- line to ground fault protection (only for type SKiiP2 GD)
- over voltage protection of the DC link voltage (optional; for SKiiP3 GD as standard)

The following chapter gives a description of the SKiiP System protection and supervisory functions as illustrated in the block diagram. The datasheets include timing and trip level data.

4.4.5.1 OCP - (O)ver (C)urrent (P)rotection and Short Circuit Protection

As shown in the block diagram SKiiP Systems feature integrated current sensors per phase leg. These current sensors can be used for AC current control. In addition they are used to protect the SKiiP System against over currents. If the AC output current is higher than the maximum permissible level of 125 % I_C (exception: SKiiP3 with AlN ceramic substrate), the IGBTs are immediately switched off and switching pulses from the controller are ignored. The error latch is set. The output ,,ERROR OUT“ is in HIGH state **Please note:** the output ,,ERROR OUT“ is an open collector output, which needs an external pull up resistor.

The over current protection reacts independently of the temperature level and provides a reliable protection of the SKiiP System.

In addition a VCEsat monitoring circuit is implemented to protect the phase leg against internal short circuit (“shoot through” protection).

4.4.5.2 Over temperature protection

The temperature of the ceramic substrate is monitored by an integrated temperature sensor. At a maximum substrate temperature of T = 115 ± 5°C the IGBTs are switched off and switching pulses from the controller are ignored. The error latch is set. The outputs ,,Overtemp. OUT“ and ,,ERROR OUT“ are in HIGH state.

Please note: the output ,,ERROR OUT“ is an open collector output which needs an external pull up resistor.

The over temperature trip threshold has been chosen at 115°C. For most air cooled applications this is sufficient to protect the system. But for water cooled systems or short time overloads the threshold might be too high. In this case the user should evaluate the analog temperature output to protect the system.

4.4.5.3 Under Voltage Protection of the Supply Voltage

The under voltage protection of the primary side monitors the internal 15V DC which is provided by the internal DC-DC converter (converts the unregulated input voltage to 15V DC) or by controlled +15V DC input (SKiiP2 only). If the under voltage trip level is reached, the IGBTs are switched off and switching pulses from the controller are ignored. The error latch is set. The output ,,ERROR OUT“ is in HIGH state. The table below gives an overview of the trip levels.

under voltage trip level @ condition	SKiiP 2	SKiiP 3
primary side, supply via 24 V pins	18,5V	no trip level
primary side, supply via 15 V pins	13,5V	-
internal regulated +15V	13,5V	13,5V
internal regulated -15V (for current sensor)	-13,5V	-13,5V
secondary side	-	10V

4.4.5.4 DC link over voltage protection

This protection is implemented for the following types:

Uzk monitoring	SKiiP 2	SKiiP 3
GD types (6 - pack)	standard	standard
GB types (2-pack)	option	-
GB types (3-pack)	option	option
GB types (4-pack)	option	option

If the operating DC link voltage is higher than VCCmax the IGBTs are turned off and switching pulses from the controller are ignored. The error latch is set. The output ,,ERROR OUT“ is in HIGH state. The trip level is given in the datasheet.

4.4.5.5 Dead Time Generation (“TOP/BOTTOM interlock”)

The interlock circuit prevents that the TOP and the BOT IGBT of one half bridge are switched on at the same time (internal short circuit). The internal interlock time is adapted to the power semiconductors, i.e. it is chosen as small as possible to allow high duty cycle but guarantees a safety margin against shoot through losses due to tail currents. The dead time does not add to a dead time given by the controller. Thus the total dead time = max (built in dead time, controller dead time). It is possible to control the SKiiP System with one switching signal and its inverted signal. No error message will be generated when overlap of switching signals occurs.

Please note that the propagation delay of the driver is the sum of interlock dead time (t_{TD}) and driver Input output signal propagation delay of the driver ($t_{d(on/off)IO}$). The dead time is only active in case that the opposite device is switching with an inverted pulse pattern.

Moreover the switching time of the IGBT chip has to be taken into account (not shown in the picture).

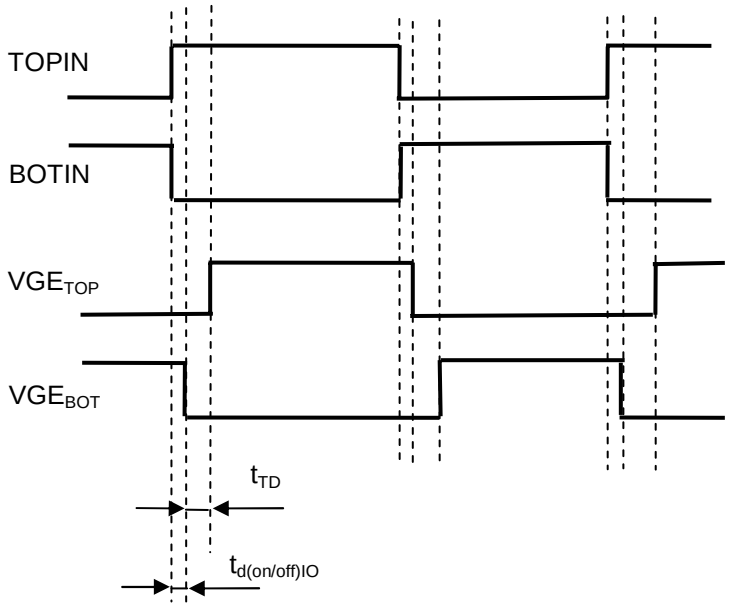


Fig. 10 Pulse Patter - dead time generation

4.4.5.6 Short Pulse Suppression

This circuit suppresses short turn-on and off-pulses. This way the IGBTs are protected against spurious noise as they can occur due to bursts on the signal lines.

Pulses shorter than 625ns are for 100% probability suppressed and all pulses longer than 750ns get through for 100% probability. Pulses with a length in-between 625ns and 750ns can be either suppressed or get through.

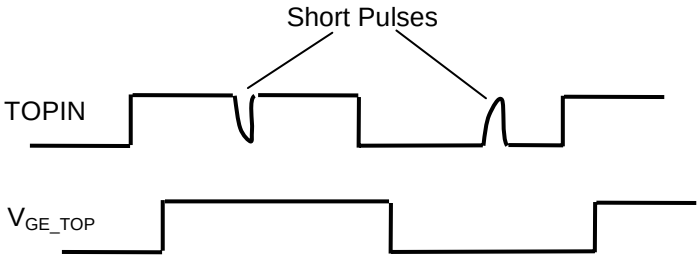


Fig. 11 Pulse Pattern - Short Pulse Suppression

4.4.5.7 Error Latch and Error Feedback

Any error detected will set the error latch and force the output ,,ERROR OUT“ into HIGH state. Switching pulses from the controller will be ignored. Reset of the error latch is only possible with no error present and all input signals in LOW state for the time Tp_{RESET} =9µs.

All logical error outputs are open collector transistors with $V_{external}$ = 3,3 - 30V / Imax=15mA. (Low signal = "no error" - wire break monitoring). We recommend to set the external pull-up voltage as high as possible.

An external pull-up resistor $R_{pull-up}$ to the controller logic high level is required. The resistor has to be in the range: $V_{external}/I_{max} < R_{pull-up} < 10k\Omega$)

Example:

for $V_{external}$ = 15V the needed resistor should be in the range $R_{pull-up}$=(15V/15mA) - 10kΩ =1kΩ-10kOhm

The external filter capacitor C_{ext} is not compulsory but for noise immunity reasons recommended. We advice to choose a value of something in the range of a few nF, because the RC time constant must not exceed the minimum error duration time of 9µs.

- For SKiiP2 the circuit can be seen in the following picture:

The circuit below illuminates the principle of the Error output for SKiiP2. The error transistor is an ordinary open collector transistor. The resistor R_{sens} acts as sensor for the short circuit protection. In case that the current exceeds the specified I_{max}=15mA the transistor will be turned off and the error signal can be detected by the customer. This way the error transistor is short circuit proof.

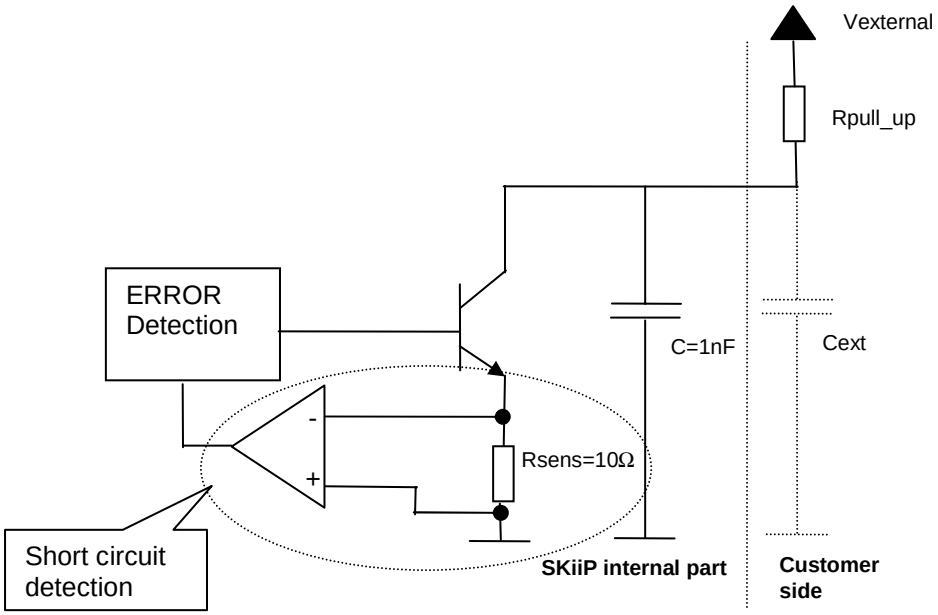


Fig. 12 SKiiP2 - Open Collector Error Transistor

- For SKiiP3 this circuit is simpler as can be seen in the following picture.

Please note: The error output of SKiiP3 is not short circuit proof.

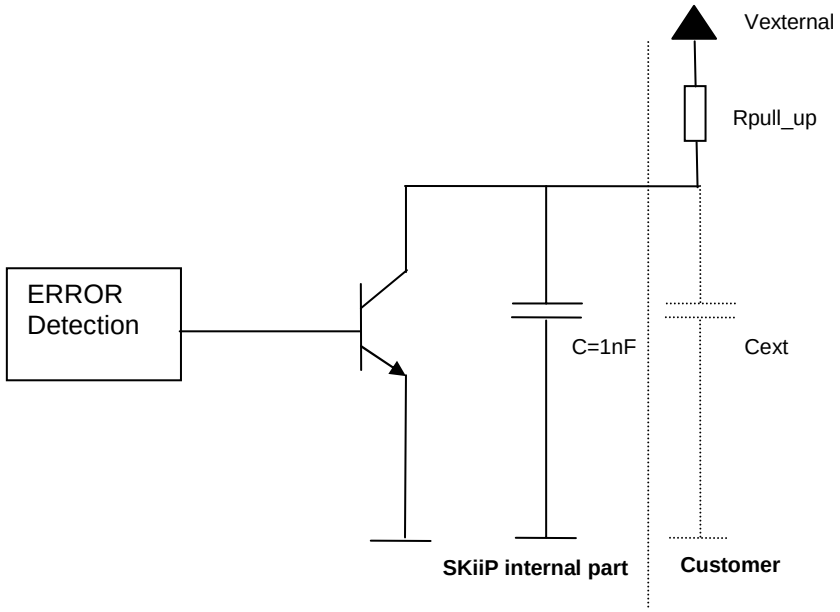


Fig. 13 SKiiP3 - Open Collector Error Transistor

4.4.5.8 Error Concept

The error management of SKiiP can be described by the following table. Any error condition will cause the error signals on the corresponding pins to go high on the open collector output (indicated by ✓).

- **Error Management of GD-Types**

	Pin 3 ERROR HB1 OUT	**Pin 6 ERROR HB2 OUT**	**Pin 9 ERROR HB3 OUT**	**Pin 11 Overtemp. OUT**
Vce-protection HB1	✓			
Vce-protection HB2		✓		
Vce-protection HB3			✓	
OCP protection HB1	✓	✓	✓	
OCP protection HB2	✓	✓	✓	
OCP protection HB3	✓	✓	✓	
temperature protection	✓	✓	✓	✓
DC-link over voltage protection	✓	✓	✓	
Ground Fault (SKiiP2 only)	✓	✓	✓	
Internal Supply Voltage Error	✓	✓	✓	

- **Error Management of GB-Types**

	Pin 3 ERROR HB1 OUT	**Pin 11 Overtemp. OUT**
Vce-protection HB1	✓	
OCP protection HB1	✓	
temperature protection	✓	✓
DC-link over voltage protection	✓	
Internal Supply Voltage Error	✓	

4.4.6 Integrated Sensor Functions

The SKiiP System features the following integrated sensors

- compensated current sensor per phase leg
- temperature sensor on ceramic substrate
- sensing of DC link voltage (optional)

4.4.6.1 Integrated Current Sensor

The SKiiP System power section integrates one current transformer per power section to measure the AC output current. The measured current is normalized to a corresponding voltage at the DIN 41651 connector. The over current trip level is set to 10V .

In all SKiiP2 and SKiiP3 systems with aluminum oxide (Al_2O_3) ceramic substrate 100% of the rated DC current I_C corresponds to 8 V and the over current trip level I_{TRIPSC} is set to 125% I_C, equivalent to 10V.

SKiiP3 Systems with aluminum nitride (AlN) ceramic substrate are from an electrical point of view similar to the same sized Al_2O_3 substrate based systems but have a better thermal conductivity and therefore a higher rated DC-current. There is no difference of the driver board (as e.g. current normalization, over current trip level etc.). For that reason both systems have the same relation between the absolute values of current and corresponding voltage. Only the relation in percent to I_C is different. Please refer to the individual datasheets for the corresponding values.

The current transformers are working according to the compensation principle. The magnetic field caused by the load current is detected by a magnetic field sensor. This is not a Hall element but a small coil with a high permeable core. Due to the properties of this sensing element there is no offset failure and almost no temperature dependence. An electronic circuit is evaluating the value of the field sensor and is feeding a current into the compensation coil thus keeping the effective magnetic field to zero. The compensation current gives an image of the load current and is evaluated across a burden resistor with an electronic circuit.

The following figure illuminates the compensation principle with the SKiiP3 current sensor. The SKiiP3 current sensor uses a switch mode controller for the compensation current versus a linear controller used in the SKiiP2 current sensor. This leads to remarkably reduced current consumption of the SKiiP3 current sensor.

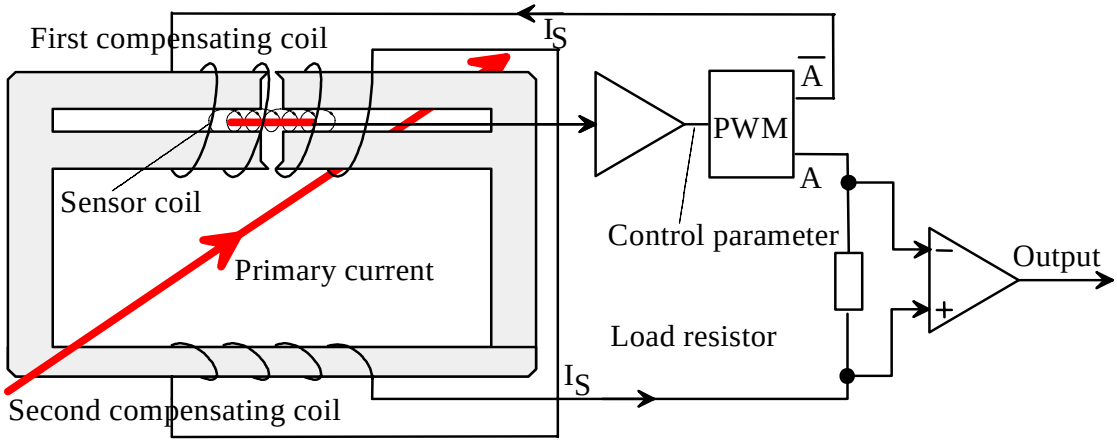


Fig. 14 SKiiP3 compensated current sensor

The table below compares the data of SKiiP current sensors (one sensor per power section).

parameter	SKiiP2	SKiiP3
continuos output current per curent sensor	$200A_{rms}$	$400A_{rms}$
continuous output current, 2s per current sensor	$250A_{rms}$	$500A_{rms}$
peak current, 10µs	3000 A	3000 A
bandwidth (-3dB)	DC - 100 kHz	DC - 50 kHz
response time	< 1µs	< 1µs
parasitic capacitance prim. - sec.	40pF	30pF

The accuracy of the current sensor depends on several points as there are:

- tolerance of current sensor electronic
- tolerance of burden resistor of current sensor
- tolerance of SKiiP internal amplification circuitry (e.g. by offset of operational amplifiers, tolerances of external passive components etc.)
- tolerance due to temperature drift

The maximum tolerance values can be calculated by the values given in the following equation:

$$\Delta I = I_C * k_{Io} + I_{actual} (k_{Ierror} - k_{Io} + |\Delta T| * TC_{Error})$$

Parameter	SKiiP2	SKiiP3
Offset k_{Io}	0,35%	0,13%
Gain Error k_{Ierror}	1,50%	1,50%
Temperature Coefficient TC_{Error}	0,001 % / K	0,002 % / K

I_C is the Nominal current per DCB

ΔI is the absolute deviation per DCB

Example:

The deviation at the current level I_{actual} =300A for a SKiiP3 (513GD172) at 85°C is (Ic = 500A):

Deviation = 500A * 0,13% + 300A * (1,5% - 0,13% + | 85°C-25°C | * 0,002% / K) = **4,76 A**

Please note that the absolute deviation is given in relationship to the current per DCB. In case that a 2-fold GB is used the deviation is the same compared to a GD type SKiiP for the same current per DCB.

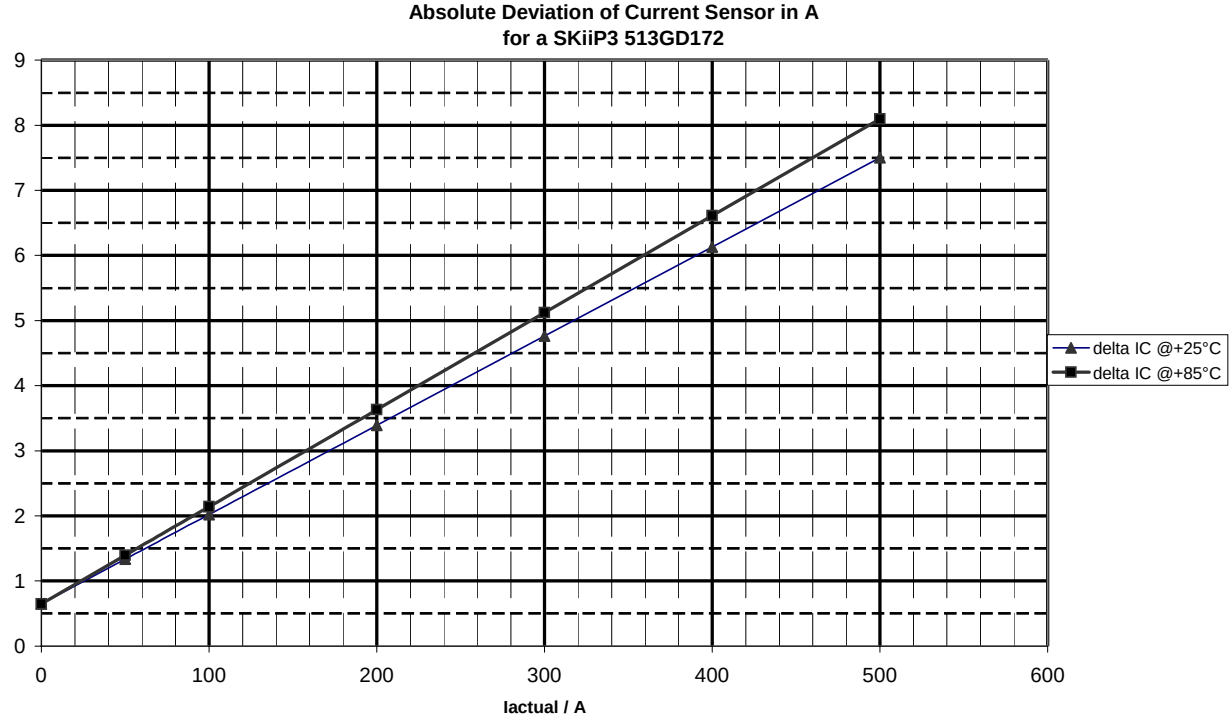


Fig. 15 Absolute Deviation of Current Sensor for a 513GD172

4.4.6.2 Integrated Temperature Sensor

The integrated temperature sensor is a semiconductor resistor with proportional characteristic (PTC characteristic). The sensor is soldered onto the ceramic substrate close to the IGBT and freewheeling diodes and indicates the actual substrate temperature. The sensor is insulated. An evaluation circuit realized on the integrated driver provides a normalized, analog voltage signal of the actual ceramic

substrate temperature value (see next Fig.) The ceramic substrate temperature is very close to the heat sink temperature.

The accuracy of the temperature sensor is approximately ± 3°C (see also the following picture). Please note that the temperature sensor is designed for T_r > 30°C. The tolerance band is very wide temperatures below 30°C.

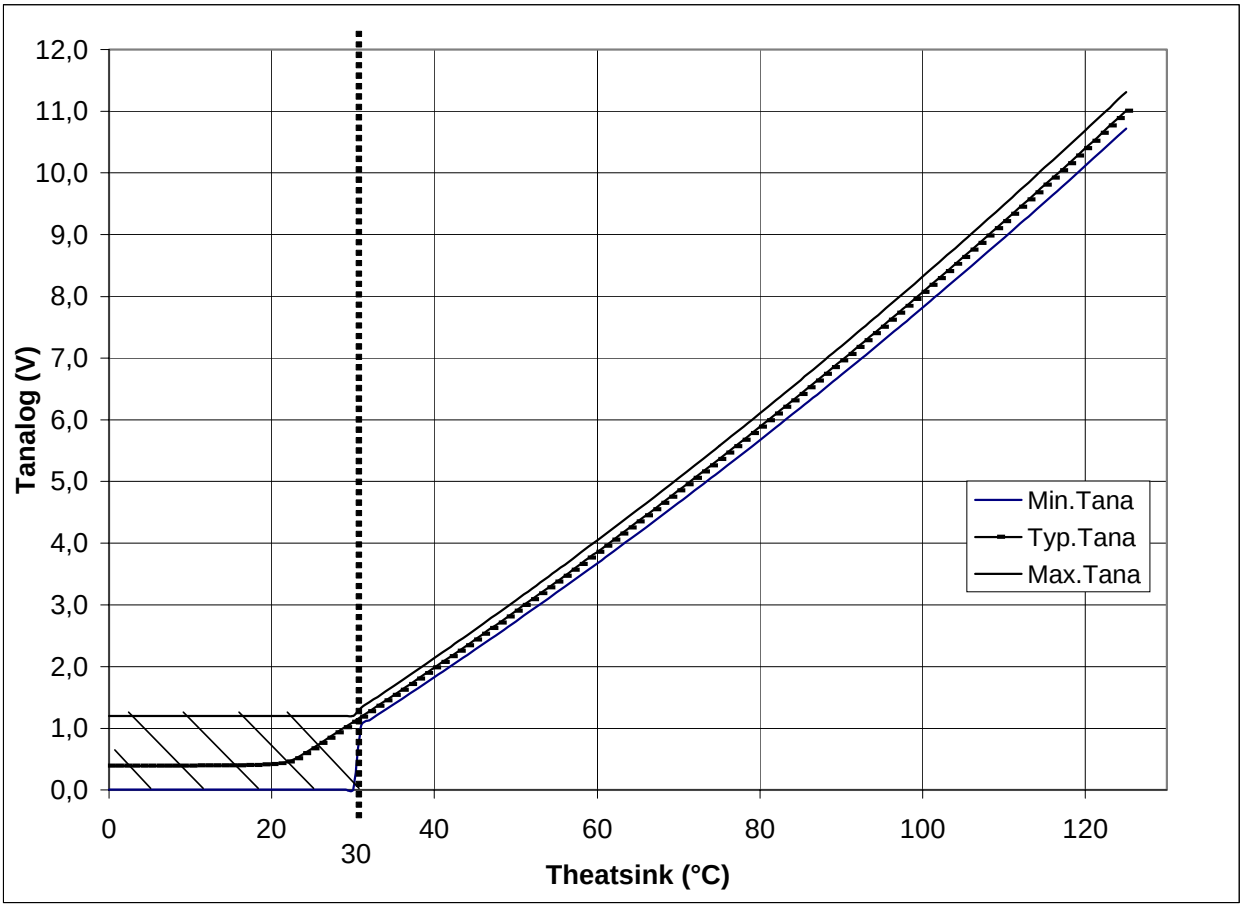


Fig. 16 Analog temperature signal $U_{analog\ OUT}$ vs. T_{sensor} : (at pin ,,Temp. analog OUT“)

4.4.6.3 Integrated DC link Voltage Monitoring

With the option U ,,analog DC-link voltage-sense“, a normalized, analog voltage signal of the actual DC-link voltage level is available at the DIN 41651 connector of the gate driver. The measurement is realized by a high impedance differential amplifier. The circuit is designed, manufactured and tested according to standard EN50178 (VDE 0160).

Normalization of the actual DC-link-voltage signal and input impedances of the measurement circuit is shown in the table below.

	SKiiP 2 and SKiiP 3		
Vces	V_{DC} ⇔ $V_{DCanalog}$	Input Impedance	V_{ccmax} ⇔ $V_{DCTripmin}$
600 V	400V ⇔ 9 V	5 MOhm	400V
1200 V	900V ⇔ 9 V	5 MOhm	900V
1700 V	1200V ⇔ 9 V	6,5 MOhm	1200V

The failure of the measured signal is ± 2% @ Ta = 25°C. The over voltage trip level is V_{ccmax}. The analog output signal $V_{DCanalogOUT}$ is filtered with a time constant of τ= 500 µs.

4.5 Brake Chopper Driver used in SKiiP2 type „GDL“

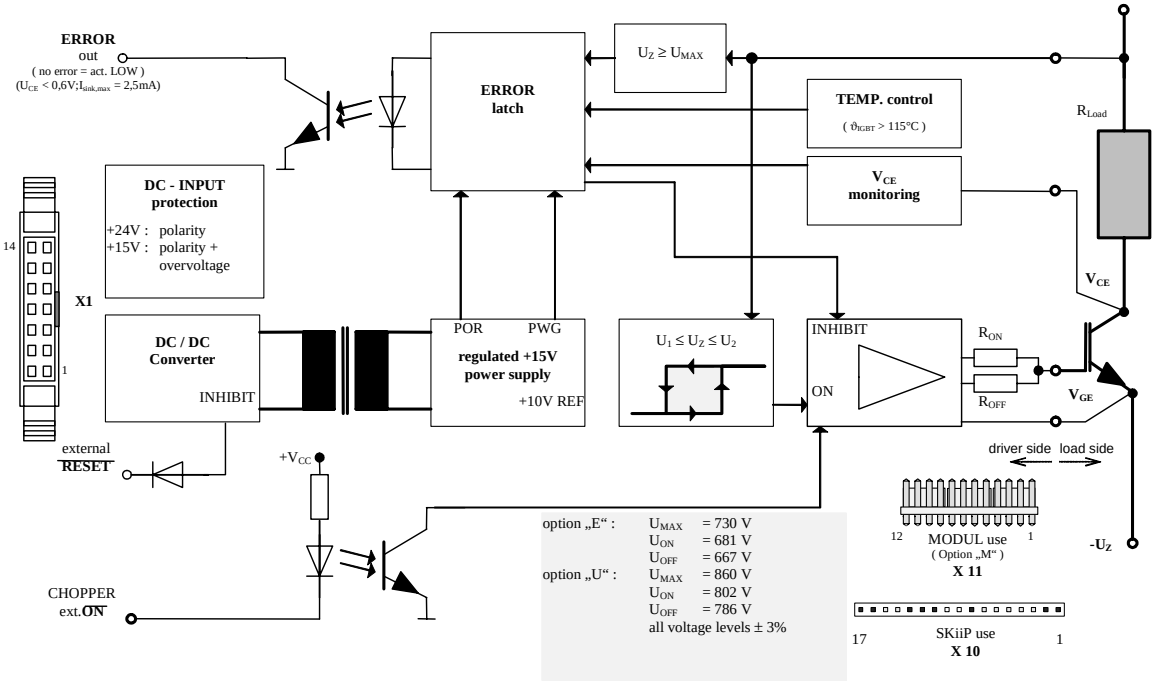


Fig. 17 Block diagram brake chopper driver

SKiiP2 GDL type incorporates a 6-pack (GD) and a brake chopper. The brake chopper of the GDL SKiiP2 is located at the right side assuming the DC terminals on the bottom.

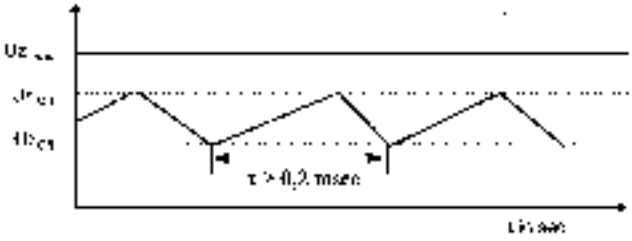
The following paragraphs explain the functionality of the brake chopper driver according to the block diagram Fig. 7:

Internal Control

The bang-bang controller generates the ON and OFF signals for the brake chopper depending on the DC link voltage level. Once the hysteresis comparator is triggered, the minimum ON time for a discharging pulse is typ. 30 µs.

Two standard versions for 1200 V SKiiP2 are available.

Type	Version E (for U_{line} = 400 V_{AC})	Version A (for U_{line} = 460 V_{AC})
UZ_{max}	730 V	860 V
UZ_{on} (Chopper On)	681 V	802 V
UZ_{off} (Chopper Off)	667 V	786 V



External Control

The input signal *CHOPPER* ext. *ON* (PIN 2) can be used for external switching (for example for discharging the DC-link capacitor while having a service). External ON switching is only possible, if the chopper's error latch is not set and does not depend on the actual value of the DC link voltage. The max. switching frequency should not exceed 5 kHz. As designed for open collector drive, this input is not depending on a certain controller logic level. Active LOW from the controller means CHOPPER = ON

Protection

- The IGBT is protected against short circuit by V_{CE}-monitoring.
- Heat sink temperature monitoring. The driver turns off at T = 115°C and the error memory is set.
- DC-voltage monitoring: If the DC voltage exceeds UZ_{max} the driver turns off and the error memory is set.

The chopper driver is protected against over voltage of the 15V supply by a suppressor diode. This suppressor diode will be destroyed in case of reverse polarity of 15 V supply. The driver is protected against reverse polarity of 24V power supply.

Error Memory

The error memory is set by various error signals. Switching ON the chopper IGBT is only possible if the error memory is in NO ERROR state. Once the error latch is set, it will remain in ERROR condition until no more error is present and input *RESET* (PIN 4) is active LOW for min. $t_{pdRESET}$ > 300 ms. After start up of power supply a power on reset takes place.

Error conditions:

a) under voltage condition of the supply voltage
   limit value when using 15 V_{DC} (± 4%): < 13,5 V
   limit value when using 24 V_{DC} (20 ... 30 V): < 16 V
b) short circuit (V_{CE} monitoring) of brake IGBT
c) DC-link over voltage: Uz > Uz_{max}
d) Over temperature: T_{chip} > 115 °C ± 5 °C

Error output

Setting of the error latch will create an error signal at the *ERROR OUT* (PIN 3). This output has an open collector transistor which is optically controlled. An external pull up resistor (max. 30 V / 2,5 mA) must be connected on the controller board to logic HIGH level. Active LOW at driver output means NO ERROR.

Power supply

The driver may be supplied either with 24 V_{DC} (20 ...30 V) or with regulated +15 V_{DC} ± 4%. If 24 V supply is used 15 V supply must not be used and vice versa.

DC / DC converter

The DC/DC converter provides an isolated power supply with low coupling capacity for the gate drive and its logic. An active LOW input at *RESET* (PIN 4) from the controller blocks the power supply for the secondary side.

4.6 Features of Standard Heat Sinks

SKiiP Systems are equipped with high performance heat sinks. The data sheets contain transient thermal data referenced to the built-in temperature sensor. This allows the calculation of junction temperature if the generated losses are known. The given thermal resistances represent worst case values.

Evaluation of thermal impedance:

junction sensor (subscript for sensor: "$_r$"): $Zth_{jr} = \Sigma Rth_{jrn} * [(1 - e^{- t / tau\ n})]$, n = 1,2,3..

sensor ambient: $Zth_{ra} = \Sigma\ Rth_{ran} * [(1 - e^{- t / tau\ n})]$, n = 1,2,3..

To simplify the comparison with other power semiconductor modules SKiiP3 data sheets also contain the thermal resistance between chip junction and heat sink (subscript for heat sink: "$_s$"). These values are given as typical values.

Please note: The reference point for heat sink temperature (subscript "$_s$") is directly below the hottest chip => the temperature of the reference point is not available in the application environment.

All technical data of SKiiP Systems are incorporated into the SEMISEL simulation software which has online access under http://www.semikron.com

For further explanations of the thermal modeling please read the SEMIKRON application hand book (also available under http://www.semikron.com).

4.6.1 Standard Heat Sink for forced Air Cooling

The drawings are available in the datasheet section. The coefficients of the transient thermal impedance are given in the data sheet (SKiiP3 only; SKiiP2 transient thermal impedances are available in a separate document). The given air volumes are valid when the SEMIKRON standard fan SKF16 is used.

Please note: Strictly speaking the given transient thermal impedance (Z_{thjr}) data are valid together with the SEMIKRON standard heat sink only. They might be adapted for other forced air cooled heat sinks which have a minimum root thickness of 14 mm.

4.6.2 Standard Heat Sink for Liquid Cooling

The drawings are available in the datasheet section. The coefficients of the transient thermal impedance are given in the data sheet. (SKiiP3 only; SKiiP2 transient thermal impedances are available in a separate document).

Please note: the given transient thermal impedance (Z_{thjr}) data are valid together with the SEMIKRON standard heat sink only and for 50%/50% water glycol cooling liquid. The usage of these value for other liquid cooled heat sinks might cause severe deviations in calculation of thermal resistance.

4.7 Options

4.7.1 U-option: DC-link Voltage Sense Monitoring

If a 2 pack SKiiP (,,GB“ type) is used with U-option the analog voltage signal of the actual DC-link value is present at Pin 12 of the driver interface instead of the signal for the actual heat sink temperature.

The 6 pack SKiiP (,,GD“ type) has DC bus bar voltage and temperature information in the standard version available.

4.7.2 F-Option: Connection to the SKiiP System using Fiber optic Interface

With the ,,option - F“ switching and error signals are transferred via fiber optic connectors. The fiber optic adapter is fixed at the cover of the SKiiP System, and connected to the integrated driver via a short flat cable. Fiber optic connectors from Hewlett Packard’s HFBR - 0501 family are in use. The receiver type HFBR 2521 (blue) is used for the input signals TOP IN (U1) and BOT IN (U3). The transmitter type HFBR 1521 (grey) is used for the output ERROR OUT (U2). Please refer to the data sheet section for exact position of the F-option.

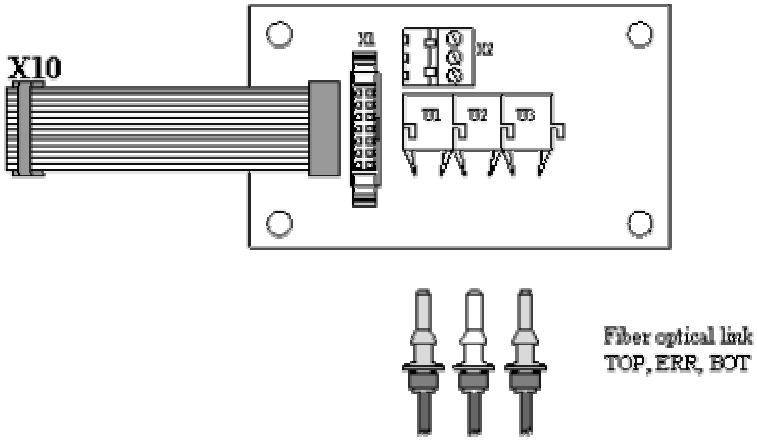


Fig. 18 Picture showing F-Option

5 Accessories

5.1 Snubber Capacitors

SEMIKRON provides film capacitors which can be adapted onto the DC-terminals of the SKiiP systems. These capacitors reduce the over voltage peak during commutation and are recommended by SEMIKRON. The table below lists the available types.

Capacitance/DC-voltage	recommended for use with	ID number
470nF / 1000V	600V, 1200V Devices	41046230
220nF / 1250V	1700V Devices	41046220

5.2 AC Busbars

The AC outputs of SKiiP GB circuits must be paralleled externally
. SEMIKRON recommends dedicated bus bars for paralleling as shown below:

Item	ID number
AC-bar for GB-Type 2-fold	41034390
AC-bar for GB-Type 3-fold	41034400
AC-bar for GB-Type 4-fold	41034410

5.3 DC-Link Capacitors and Bus Bars

SEMIKRON supplies tested capacitors banks with low stray inductance for direct mounting onto the SKiiP. You can make a choice from the following most common references:

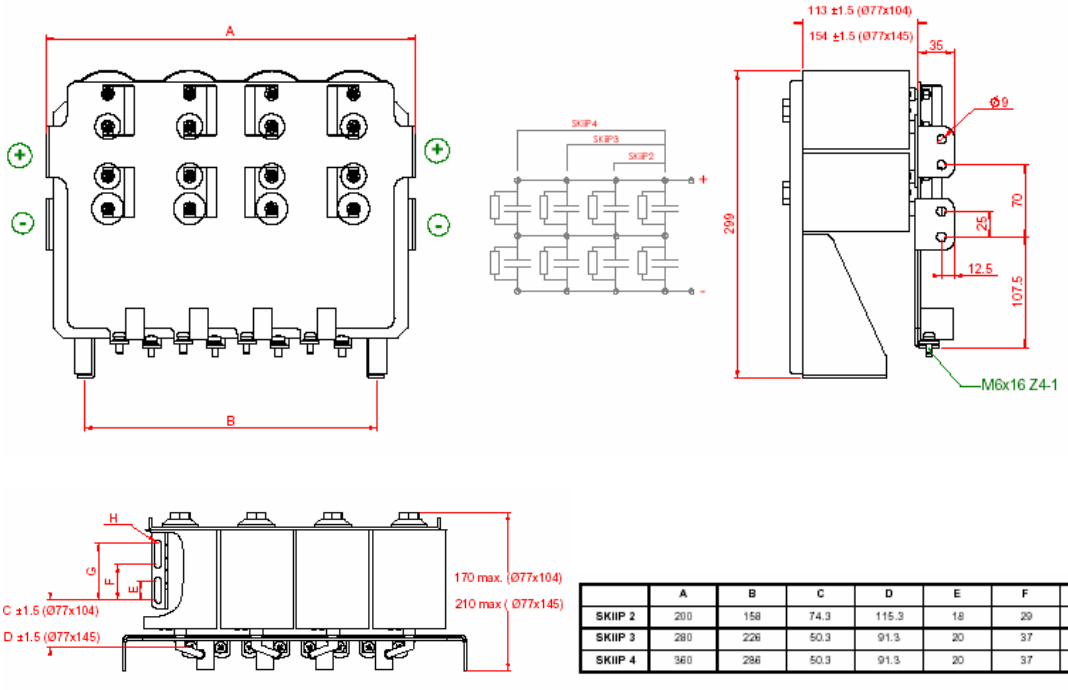
		Rated capacitance (µF)	Ripple current (A) (max, 100hz,	Code Désignation	Rated voltage (V)	Surge voltage 30s (V)
Skiip IGBT 1200V Fig 19	2-fold	2200	17,6	SKCB 2m2-45-2-12	800 V	900V
	3-fold	3300	26,4	SKCB 2m2-45-3-12		
	4-fold	4400	35,2	SKCB 2m2-45-4-12		
	2-fold	3300	23,6	SKCB 3m3-45-2-12		
	3-fold	5000	35,4	SKCB 3m3-45-3-12		
	4-fold	6600	47,2	SKCB 3m3-45-4-12		
	2-fold	4700	26,8	SKCB 4m7-40-2-12	720V	800V
	3-fold	7000	40,2	SKCB 4m7-40-3-12		
	4-fold	9400	53,6	SKCB 4m7-40-4-12		
Skiip IGBT 1700V Fig 20	2-fold	1500	17,6	SKCB 2m2-45-2-17	1250V	1350V
	3-fold	2200	26,4	SKCB 2m2-45-3-17		
	4-fold	2900	35,2	SKCB 2m2-45-4-17		
	2-fold	2200	23,6	SKCB 3m3-45-2-17		
	3-fold	3300	35,4	SKCB 3m3-45-3-17		
	4-fold	4400	4,2	SKCB 3m3-45-4-17		
	2-fold	3100	26,8	SKCB 4m7-40-2-17	1050V	1200V
	3-fold	4700	40,2	SKCB 4m7-40-3-17		
	4-fold	6300	53,6	SKCB 4m7-40-4-17		

SEMIKRON electrolytic capacitors have been specified for a drive application usage. Please check the current in the capacitors for your own application before making a choice.

The following table gives the maximum ripple current per capacitor bank at 100Hz, 85°C, for 15 000 hours life time.

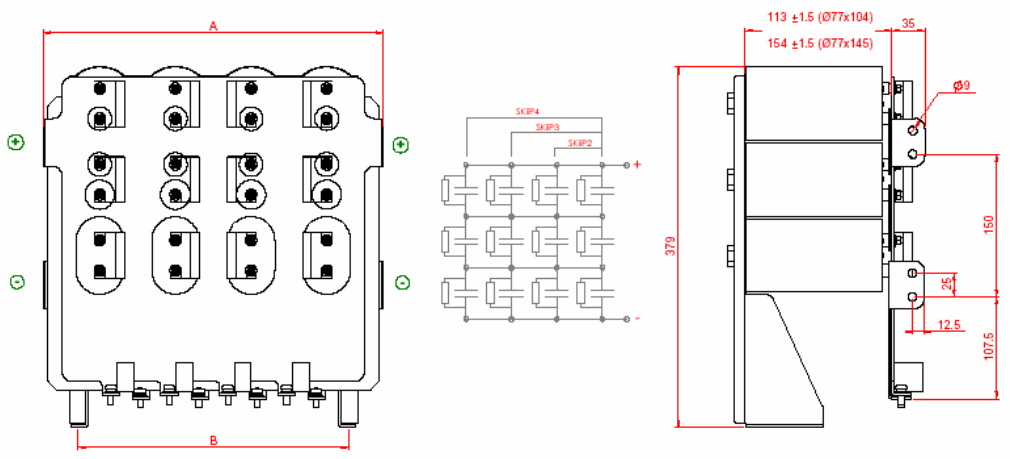
Voltage	Rated capacitance (µF)	Ripple current (A) (max, 100hz, 85°c)
350	3300	10,9
400	2200	8,2
400	3300	10,1
400	4700	13,4
450	2200	8,8
450	3300	12,6
450	4700	14

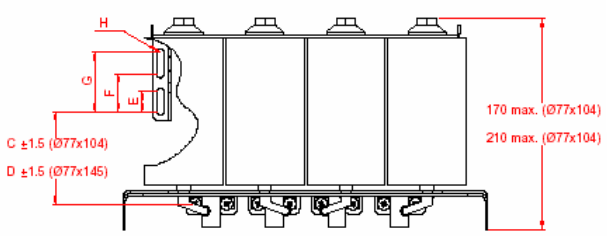
The capacitor bank comes along with a reinforced support plate and the snubber capacitors. During assembly, great care should be taken to avoid any damage onto the sharing resistors.



	A	B	C	D	E	F	G	H
SKIIP 2	200	158	74.3	115.3	18	29	43	R 2.75
SKIIP 3	280	226	50.3	91.3	20	37	59	R 3.5
SKIIP 4	360	286	50.3	91.3	20	37	59	R 3.5

Fig. 19 DC Link Capacitor Bank for 1200V IGBTs





	A	B	C	D	E	F	G	H
SKIIP 2	200	158	74.3	115.3	18	29	43	R 2.75
SKIIP 3	280	226	50.3	91.3	20	37	59	R 3.5
SKIIP 4	360	286	50.3	91.3	20	37	59	R 3.5

Fig. 20 DC Link Capacitor Bank for 1700V IGBTs

For further details on capacitor banks see also the separate capacitor datasheets.

6 Application instructions

6.1 ESD Protection

Every SKiiP System is equipped with an ESD protective cover. To avoid any electrostatic discharge do not remove the protective cover before the SKiiP System is completely installed. Use conductive floor and grounded armbands during assembly.

6.2 Connections to power terminals

It is mandatory to use a laminated low-inductive bus bar structure to connect the DC link to the DC-terminals of the SKiiP System. The DC link bank has to be designed this way that each DCB faces the same impedance to the voltage source respectively DC link bank. This way the current distribution is as even distributed as possible. The usage of high frequency film capacitors (see also section accessories) on the DC link connections is necessary, to reduce the over voltages in case of a short circuit.

When a “GB” -type SKiiP System is used the AC terminals must be connected to each other. SEMIKRON provides suitable bus bars (see section accessories”). And again the AC terminals have to be connected as symmetric as possible to ensure the even current distribution.

Furthermore any control signals shall be kept as far away as possible from the DC link rail (because of high dv/dt on the AC rails and high di/dt on the DC rails).

The torque level for DC and AC terminal screws as well as thread geometry is given in the datasheets. The applied pulling forces in any direction on the terminals must be kept to a minimum. For that reason it is compulsory to take measures to reduce these forces. We recommend using fixing posts to relieve the strain on the AC terminals. The posts shall be mounted directly onto the heat sink. Forces caused by the dc link capacitor bank have to be absorbed by the mechanical construction. Both measures have the purpose to absorb any stresses from external parts to the terminals (e.g. the dc link capacitors or heavy AC cables). Please keep the fixing posts as close as possible to the module.

The SKiiP System can be mounted in any position.

The rating and cooling of the cable must be carried out in that way that no thermal energy is fed into the SKiiPPACK. For that reason the terminal temperature on the AC terminals shall not exceed 115°C at $400A_{rms}$ and 70°C heat sink temperature. For the dc link terminals the temperature shall not exceed 115°C at $280A_{rms}$ and 70°C heat sink temperature.

The AC outlet of SKiiP3 has a different position compared to SKiiP2; please refer to the data sheet for exact position.

6.3 Connection to the Signal Terminals of the Gate Driver

The standard connection to a SKiiP System is done via a DIN 41651 connector. Because of voltage drop and for immunity against electromagnetic interference the maximum length of the flat cable should not exceed 3 meters. To avoid interferences, the flat cable should be placed as far as possible away from the power terminals, the power cables, the DC-link capacitors and all other noise sources. We recommend to keep the ribbon cables as close to GND as possible (e.g. heat sink or the like).

Because of the EMC conception of the driver board the usage of expensive screened flat ribbon cables is in many applications not needed. However in very noise intensive applications the noise immunity can be improved by screened cable.

6.4 Environmental Restrictions

Humidity and climate class are shown in the data sheets. The documented classes specify the restrictions for operation, storage and transport of SKiiP Systems.

6.5 Parallel Operation of „GB“-type SKiiP Systems

In applications where paralleling of 2,3 or more GB type SKiiP systems is necessary, it has to be made sure that no in-homogenous current distribution occurs. The reasons for this can be:

- different propagation time of driver boards (jitter of approx. 0...150ns)
- different switching times of devices (due to different Vge - thresholds)
- tolerance of forward voltage drop of diodes *
- tolerance of forward voltage drop of IGBTs
- no symmetric AC bus bar layout
- different cooling conditions of paralleled half bridges (e.g. in air cooled applications with thermal stacking)

* For paralleling of „GB“-type SKiiP Systems, equal SKiiP System with equal V_f group must be used.

Please note: the on state voltage of the freewheeling diode of each „GB“-type SKiiP system is classified in Vf-groups to avoid inhomogeneous current distribution within the paralleled dies. The Vf group of a „GB“-type SKiiP System can be identified on the label.

The system designer has to make sure that there is sufficient inductance (a few µH should be in most applications sufficient) between the AC output terminals of the 2 paralleled „GB“-type SKiiP Systems to avoid inhomogeneous current distribution.

L might be realized by iron powder ferrites (e.g. COROVAC). The required inductance depends on DC voltage, allowable “cross” current and the propagation time differences of the paralleled “GB”-type SKiiP Systems.

For a maximum deviation of the maximum rated output current the inductance has to be rated with a minimum value as shown in the picture below.

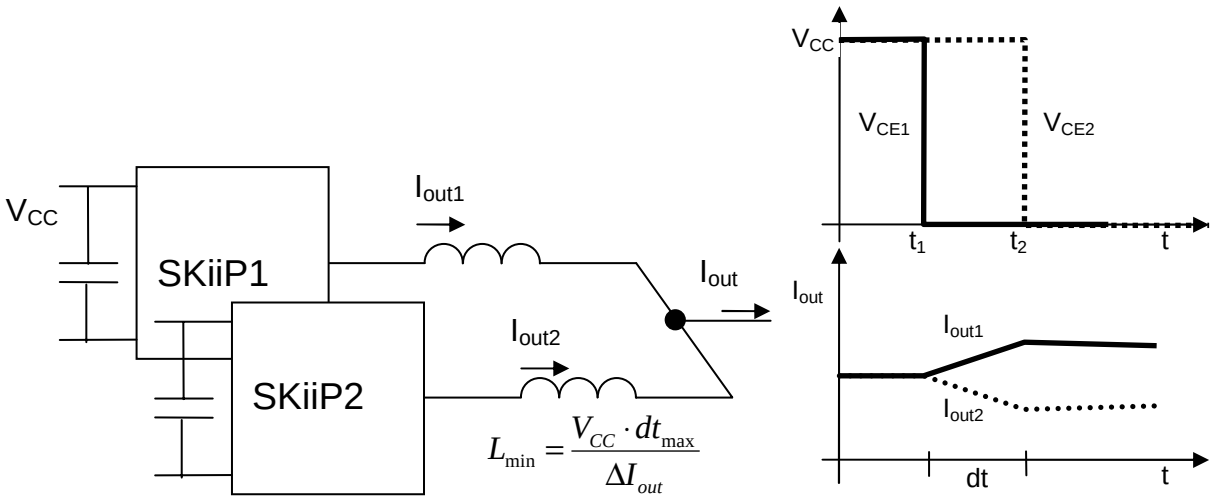


Fig. 21 Paralleled SKiiPs

Thus in an application with V_{CC}= 900V, I_{outmax}=2x600A=1200A, a permissible current deviation of 10% of the overall current the minimum value of the inductor is:

$$L_{min} = \frac{900V * 150ns}{10\% * 1200A} = 1{,}1\mu H$$

It has to be taken into account that for in-homogenous current sharing the power modules have to be de-rated (e.g. in the case above 1200A output current are needed, thus the modules have to be rated for the (600A each + 10%* 1200A) = 720A).

6.6 Electro-Magnetic Interference

The EMI relevant behavior is determined by the switching behavior on the one hand and on the coupling characteristic to the surrounding environment on the other hand (see also application handbook).

With SKiiP3 a new generation of silicon is introduced, which reduces the total loss per ampere output current compared to SKiiP2 and therefore shows different switching characteristics versus SKiiP2. This must be taken into account when SKiiP2 is replaced by SKiiP3.

The ceramic substrate area of SKiiP3 is increased towards SKiiP2. Therefore the capacitive coupling between heat sink and SKiiP3 is higher (please refer to data sheet parameter C_{CHC}).

The coupling capacitance of SKiiP between the driver primary and secondary side is determined by the signal and the DCDC transformers. The values can be seen in the following table.

	GD	GB
$C_{prim-sec}$	3x10pF	2x10pF

6.7 Usage of Water Cooled Heat Sinks

For the usage of water cooled heat sinks we recommend to take care of the following points:

- Always ensure to use the correct concentration of cooling liquid (for details see data sheet). In case that the concentration of corrosion-inhibitors is too low, corrosion as consequential damage may occur.
- Never leave cooling liquid in heat sinks which are temporarily not in use. This can lead to corrosion as consequential damage on parts which become wet due to humidity.
- Please ensure that the cooling liquid is suitable for all metal parts in the cooling circuit (e.g. steel, aluminum, other non-ferrous metals)
- Use only water which has been de-ionized (e.g. chlorine ions can accelerate the corrosion)
- The water hardness shall be kept to a minimum, to avoid scale. Please not that scale increase the thermal resistance.
- The O_2 content has to be kept to a minimum by a closed cooling circuit to avoid corrosion.

6.8 Further Application Support

For electrical and thermal design support please use SEMISEL. under SEMIKRON website http://semisel.semikron.com or read the SEMIKRON application hand book (also available under http://www.semikron.com).