

Octal channel high side driver

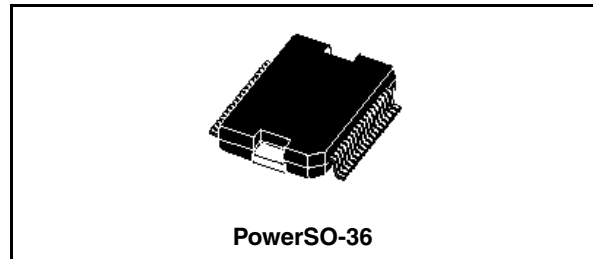
Features

Type	$R_{DS(on)}$	I_{out}	V_{CC}
VN808-E	150m Ω	0.7A	45V

- $V_{CC}/2$ compatible input
- Junction over-temperature protection
- Case over-temperature protection for thermal independence of the channels
- Current limitation
- Shorted load protection
- Undervoltage shutdown
- Protection against loss of ground
- Very low stand-by current
- Compliance to 61000-4-4 IEC test up to 4KV

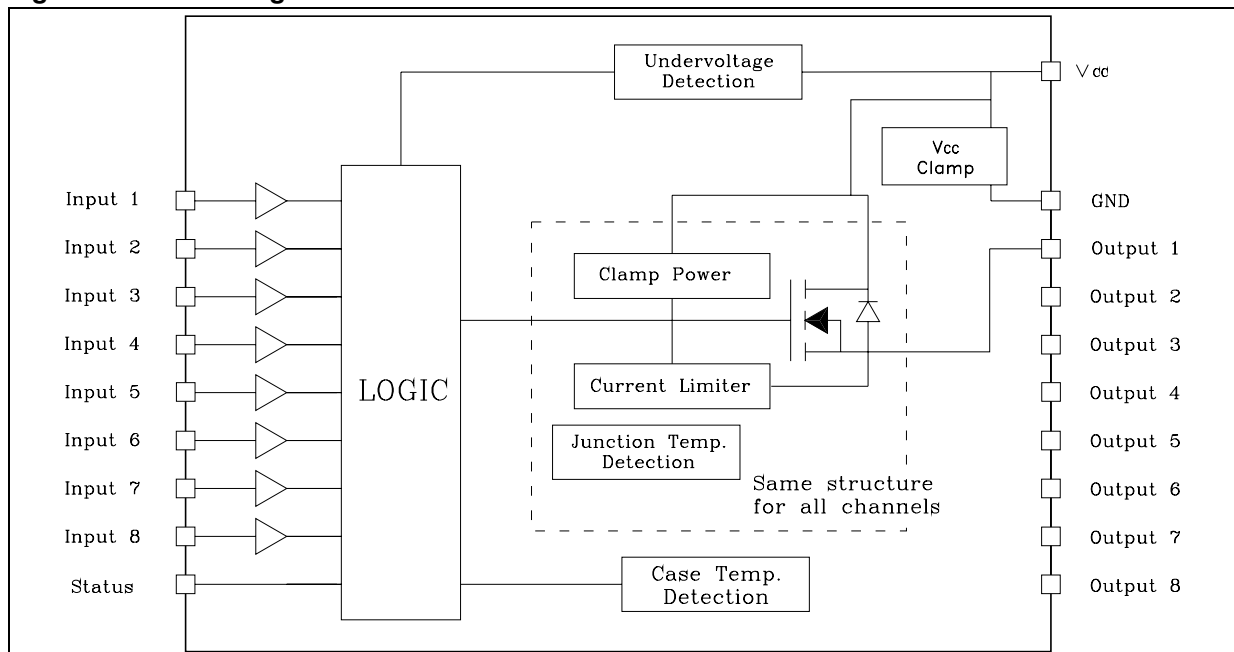
Description

The VN808-E is a monolithic device designed in STMicroelectronics VIPower M0-3 technology, intended for driving any kind of load with one side connected to ground.



Active current limitation combined with thermal shutdown and automatic restart, protect the device against overload. In overload condition, channel turns OFF and back ON automatically so as to maintain junction temperature between T_{TSD} and T_R . If this condition makes case temperature reach T_{CSD} , overloaded channel is turned OFF and will restart only when case temperature has decreased down to T_{CR} (see waveform 3 [Figure 8 on page 11](#)). Non overloaded channels continue to operate normally. Device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for industrial applications conform to IEC 61131

Figure 1. Block diagram



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1 Maximum ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	45	V
$-I_{GND}$	DC ground pin reverse current TRAN Ground pin reverse current (pulse duration < 1ms)	-250 -6	mA A
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-2	A
I_{IN}	DC Input current	± 10	mA
V_{IN}	Input voltage range	$-3/+V_{CC}$	V
V_{ESD}	Electrostatic discharge (R = 1.5K Ω ; C = 100pF)	2000	V
P_{TOT}	Power dissipation at $T_C = 25^\circ\text{C}$	96	W
L_{MAX}	Max inductive load ($V_{CC} = 24\text{V}$, $R_{LOAD} = 48\Omega$, $T_A = 100^\circ\text{C}$)	2	H
T_J	Junction operating temperature	Internally limited	$^\circ\text{C}$
T_C	Case operating temperature	Internally limited	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	$^\circ\text{C}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	Max 1.3	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction-ambient ⁽¹⁾	Max 50	$^\circ\text{C}/\text{W}$

1. When mounted on FR4 printed circuit board with 0.5cm² of copper area (at least 35 μm thick) connected to all TAB pins.

2 Electrical characteristics

($10.5V < V_{CC} < 32V$; $-40^{\circ}C < T_J < 125^{\circ}C$; unless otherwise specified)

Table 3. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		10.5		45	V
V_{USD}	Undervoltage shutdown		7		10.5	V
R_{ON}	On state resistance	$I_{OUT} = 0.5A$; $T_J = 25^{\circ}C$ $I_{OUT} = 0.5A$;		150	185 280	m Ω m Ω
I_S	Supply current	OFF state; $V_{CC} = 24V$; $T_{CASE} = 25^{\circ}C$ ON state(all channels ON); $V_{CC} = 24V$, $T_{CASE} = 100^{\circ}C$			150 12	μA mA
I_{LGND}	Output current at turn-off	$V_{CC} = V_{STAT} = V_{IN} = V_{GND} = 24V$ $V_{OUT} = 0V$			1	mA
$I_{L(off)}$	OFF state output current	$V_{IN} = V_{OUT} = 0V$;	0		5	μA
$V_{OUT(off)}$	OFF state output voltage	$V_{IN} = 0V$, $I_{OUT} = 0A$			3	V
$t_d(V_{CCon})$	Power-on delay time from V_{CC} rising edge	Table 7.		1		ms

Table 4. Switching ($V_{CC} = 24V$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{ON}	Turn-on time	$R_L = 48\Omega$ from 80% V_{OUT} Figure 6.		50	100	μs
t_{OFF}	Turn-off time	$R_L = 48\Omega$ to 10% V_{OUT} Figure 6.		75	150	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 48\Omega$ from $V_{OUT} = 2.4V$ to $V_{OUT} = 19.2V$ Figure 6.		0.7		V/ μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 48\Omega$ from $V_{OUT} = 21.6V$ to $V_{OUT} = 2.4V$ Figure 6.		1.5		V/ μs

Table 5. Input pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{INL}	Input low level				$V_{CC}/2-1$	V
I_{INL}	Low level input current	$V_{IN} = V_{CC}/2 - 1V$	80			μA
V_{INH}	Input high level		$V_{CC}/2+1$			V
I_{INH}	High level input current	$V_{IN} = V_{CC}/2 + 1V$		150	260	μA
$V_{I(HYST)}$	Input hysteresis voltage			0.6		V
I_{IN}	Input current	$V_{IN} = V_{CC} = 32V$			300	μA

Table 6. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{CSD}	Case shut-down temperature		125	130	135	$^{\circ}C$
T_{CR}	Case reset temperature		110			$^{\circ}C$
T_{CHYST}	Case thermal hysteresis		7	15		$^{\circ}C$
T_{TSD}	Junction shutdown temperature		150	175	200	$^{\circ}C$
T_R	Junction reset temperature		135			$^{\circ}C$
T_{HYST}	Junction thermal hysteresis		7	15		$^{\circ}C$
I_{lim}	DC Short circuit current	$V_{CC} = 24V; R_{LOAD} = 10m\Omega$	0.7		1.7	A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 0.5A; L = 6mH$	$V_{CC}-57$	$V_{CC}-52$	$V_{CC}-47$	V

Table 7. Status pin

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{HSTAT}	High level output current	$V_{CC} = 18...32V; R_{STAT} = 1K\Omega$ (Fault condition)	2	3	4	mA
I_{LSTAT}	Leakage current	Normal operation; $V_{CC} = 32V$			0.1	μA
V_{CLSTAT}	Clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6.0	6.8 -0.7	8.0	V V

3 Pin connections

Figure 2. Connection diagram (top view)



Table 8. Pin functions

Pin N°	Symbol	Function
TAB	V _{CC}	Positive power supply voltage
1	V _{CC}	Positive power supply voltage
2,3,4,5	NC	Not connected
6	Input 1	Input of channel 1
7	Input 2	Input of channel 2
8	Input 3	Input of channel 3
9	Input 4	Input of channel 4
10	Input 5	Input of channel 5
11	Input 6	Input of channel 6
12	Input 7	Input of channel 7
13	Input 8	Input of channel 8
14,15,16,17,18	NC	Not connected
19	GND	Logic ground
20	STATUS	Common open source diagnostic for over-temperature
21,22	Output 8	High-Side output of channel 8
23,24	Output 7	High-Side output of channel 7

Table 8. Pin functions (continued)

Pin N°	Symbol	Function
25,26	Output 6	High-Side output of channel 6
27,28	Output 5	High-Side output of channel 5
29,30	Output 4	High-Side output of channel 4
31,32	Output 3	High-Side output of channel 3
33,34	Output 2	High-Side output of channel 2
35,36	Output 1	High-Side output of channel 1

4 Current, voltage conventions and internal diagram

Figure 3. Current and voltage conventions

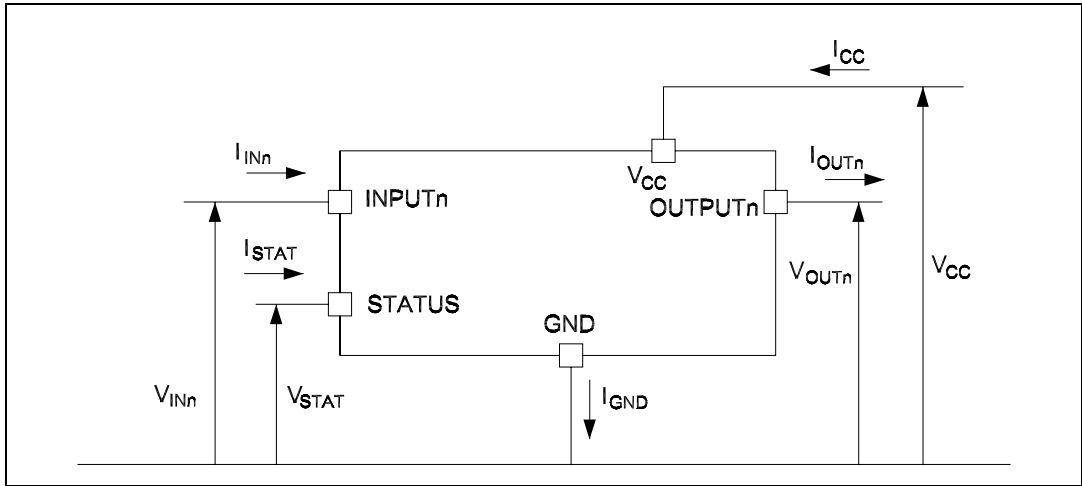


Figure 4. Equivalent internal block diagram (same structure for all channel)

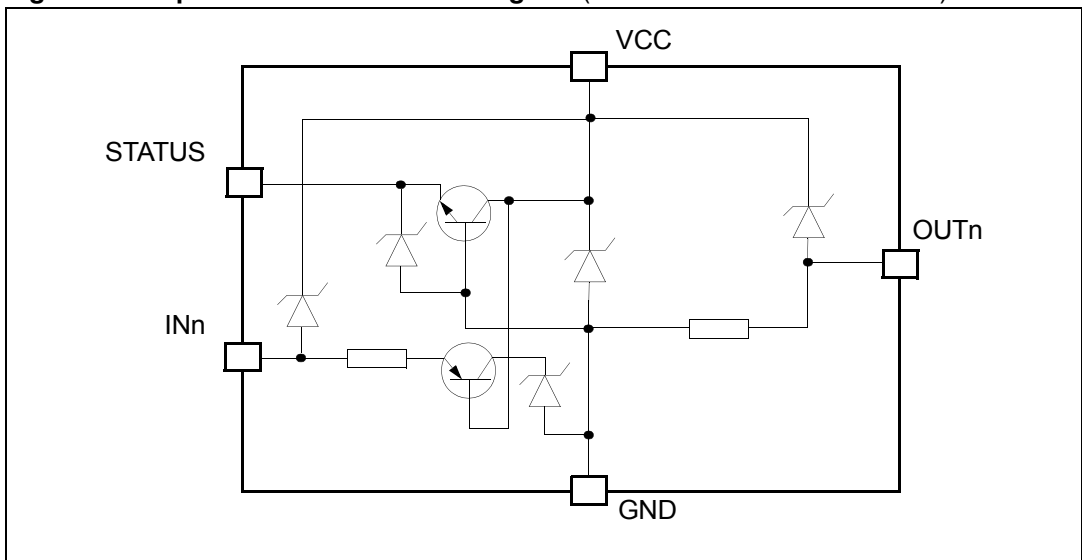


Figure 5. Application example

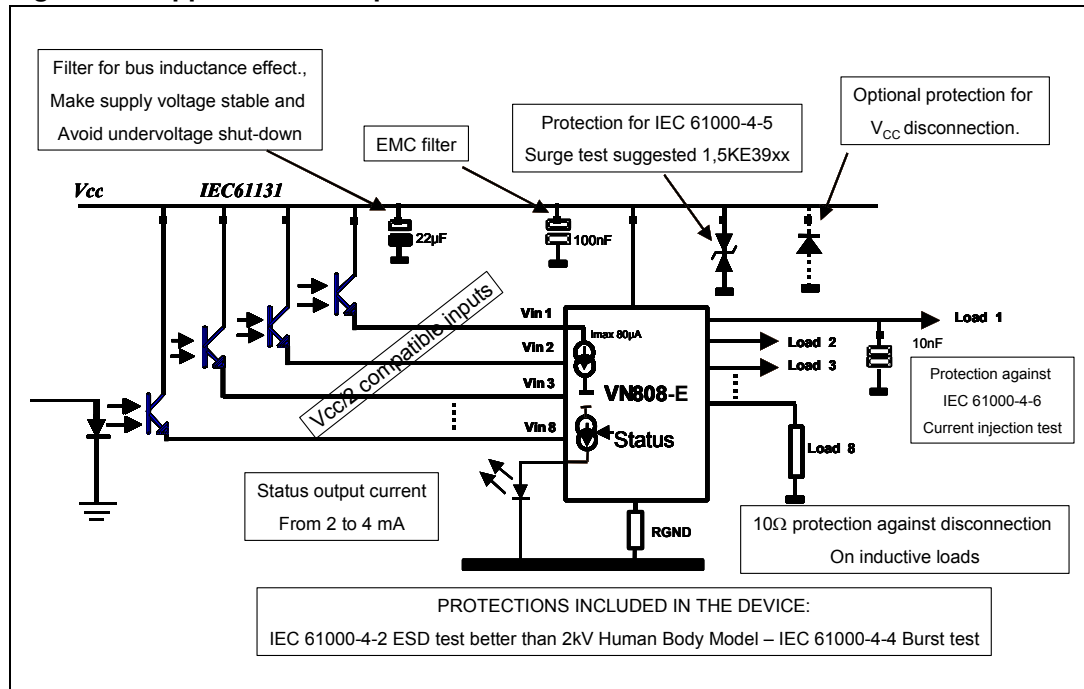


Table 9. Truth table

Conditions	INPUTn	OUTPUTn	STATUS
Normal operation	L H	L H	L L
Current limitation	L H	L X	L L
Overtemperature (see waveforms 3, 4 Figure 8) -> $T_J > T_{TSD}$	L H	L L	L H
Undervoltage	L H	L L	X X

5 Switching time waveforms

Figure 6. Turn-ON & turn-OFF

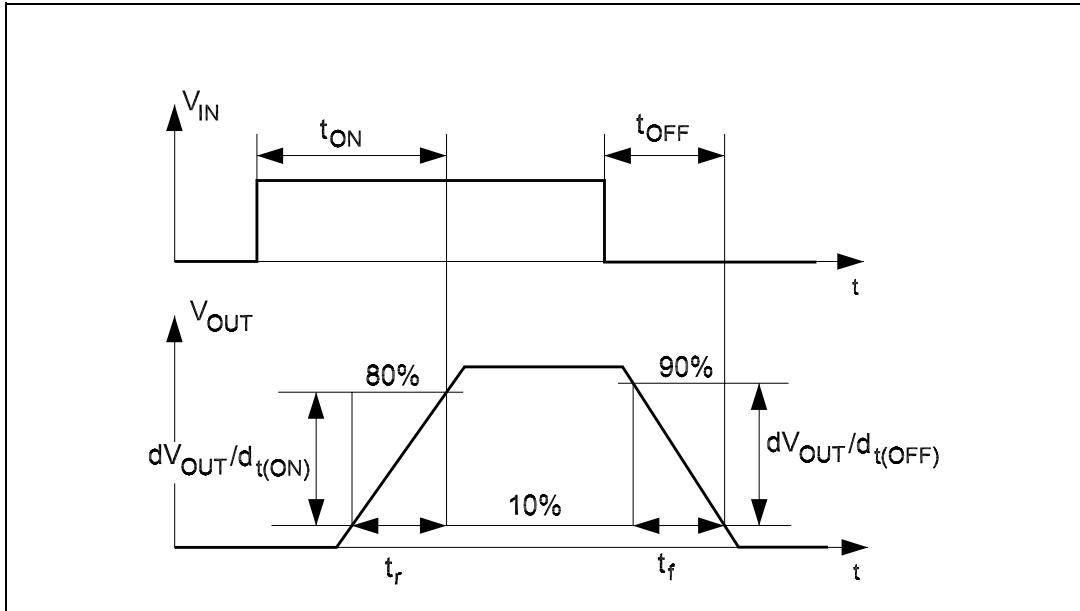


Figure 7. V_{CC} turn-ON

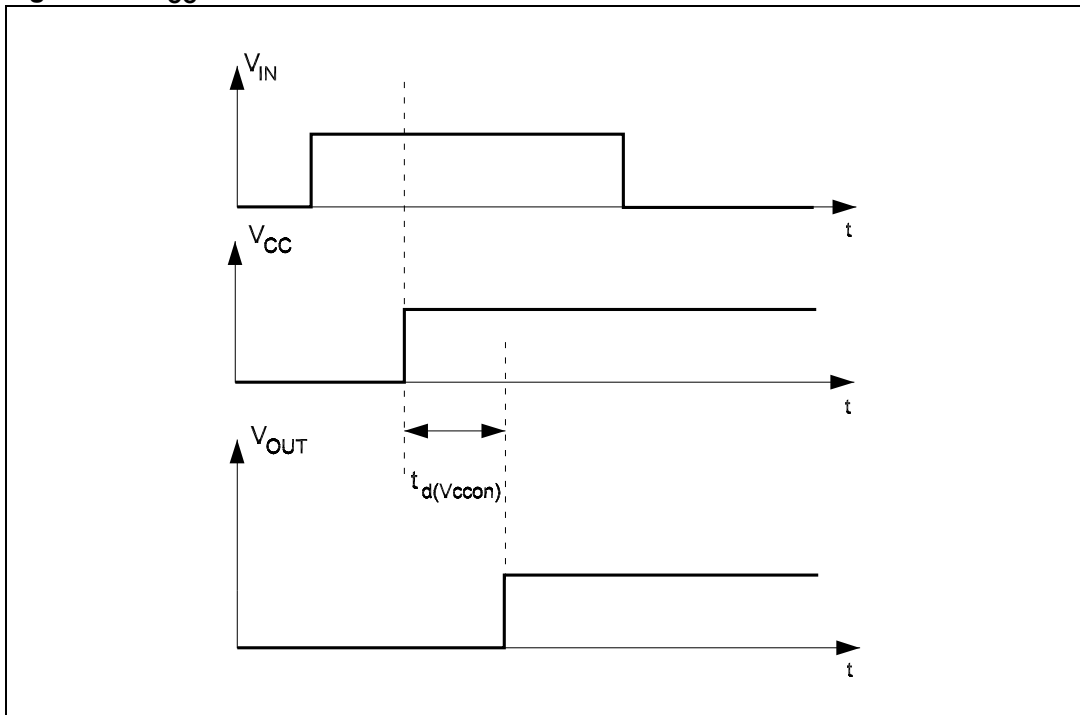


Figure 8. Waveforms

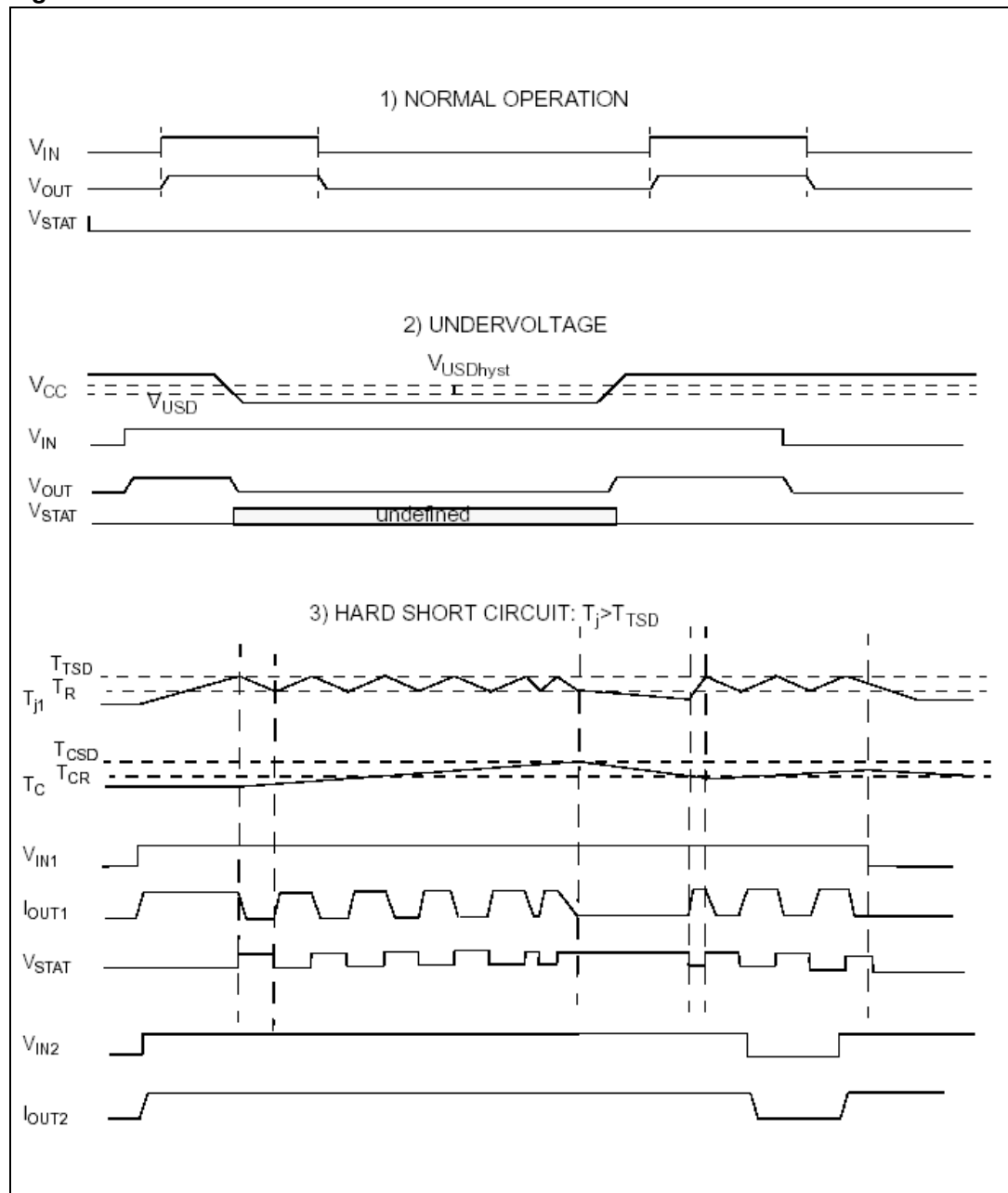
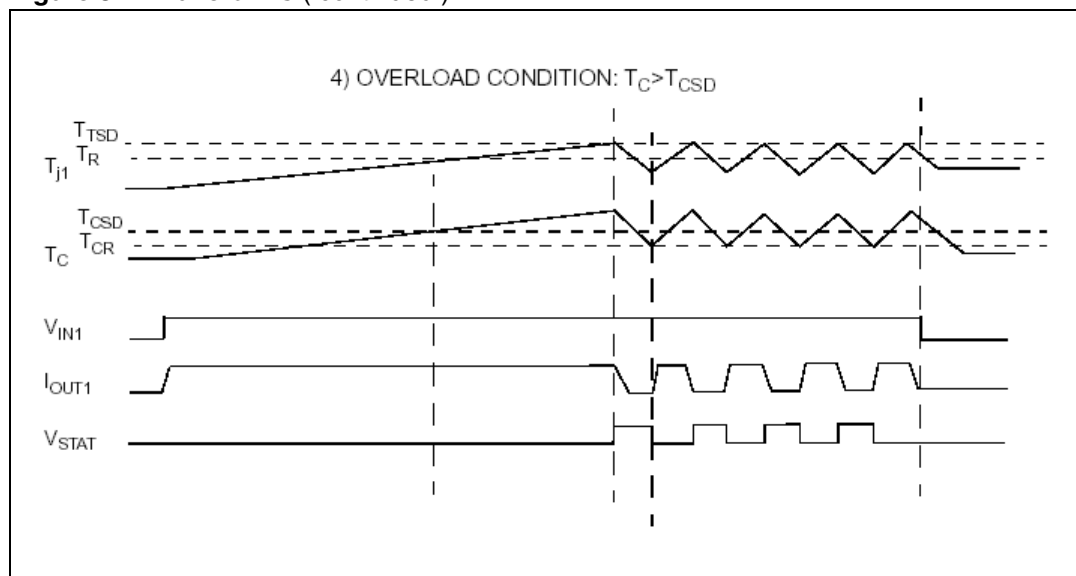


Figure 8. Waveforms (continued)



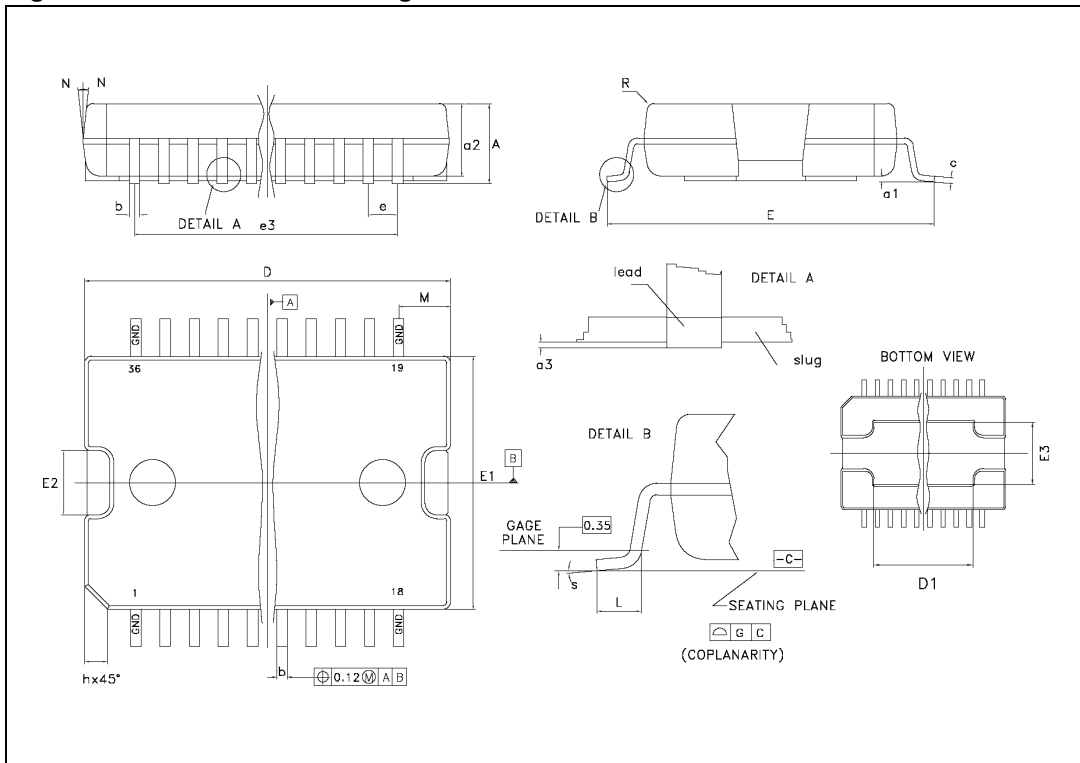
6 Mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 10. PowerSO-36 Mechanical Data

Dimensions						
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			3.60			0.1417
a1	0.10		0.30	0.003		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.22		0.38	0.008		0.0150
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.622		0.6299
D1	9.40		9.80	0.370		0.3858
E	13.90		14.50	0.547		0.5709
E1 (1)	10.90		11.10	0.429		0.4370
E2			2.90			0.1142
E3	5.8		6.2	0.228		0.2441
e		0.65			0.025	
e3		11.05			0.435	
G	0		0.10	0.000		0.0039
H	15.50		15.90	0.610		0.6260
h			1.10			0.0433
L	0.80		1.10	0.031		0.0433
N			10°			10°
S	0°		8°	0°		8°

Figure 9. PowerSO-36 drawings



7 Order codes

Table 11. Order codes

Part number	Package	Packaging
VN808-E	PowerSO-36	Tube
VN808TR-E	PowerSO-36	Tape and reel

8 Revision history

Table 12. Revision history

Date	Revision	Changes
13-Sep-2005	1	Initial release
1-Mar-2007	2	Document reformatted
12-Mar-2007	3	Typo in <i>Figure 3</i> .
26-Mar-2007	4	Typo note <i>Table 2</i> .

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