PRELIMINARY

SERIAL I/O REAL TIME CLOCK WITH WAKE-UP OUTPUT

■ GENERAL DESCRIPTION

The NJU6358 series is a serial I/O Real Time Clock with wake-up output suitable for 4-bit microprocessor.

It contains quartz crystal oscillator, counter, shift register, alarm register, voltage regulator, internal and external voltage detector and interface controller.

The NJU6358 requires only 4-port of microprocessor for data transmission, and the crystal for the watch.

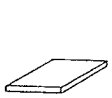
The operating voltage is allowed at both of 5V and 3V, and the clock operation is available on 2V.

The output timing of the wake-up can be selected the true time or the period.

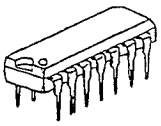
The internal voltage detector detects the drop of the power supply and the external voltage detector is useful for any voltage detection independently.

Furthermore, the long time back up is available as the current consumption during the back up period is a few.

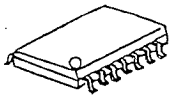
■ PACKAGE OUTLINE



NJU6358C



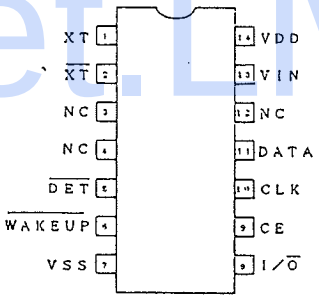
NJU6358D



NJU6358M

NJU6358V

■ PIN CONFIGURATION



■ FEATURES

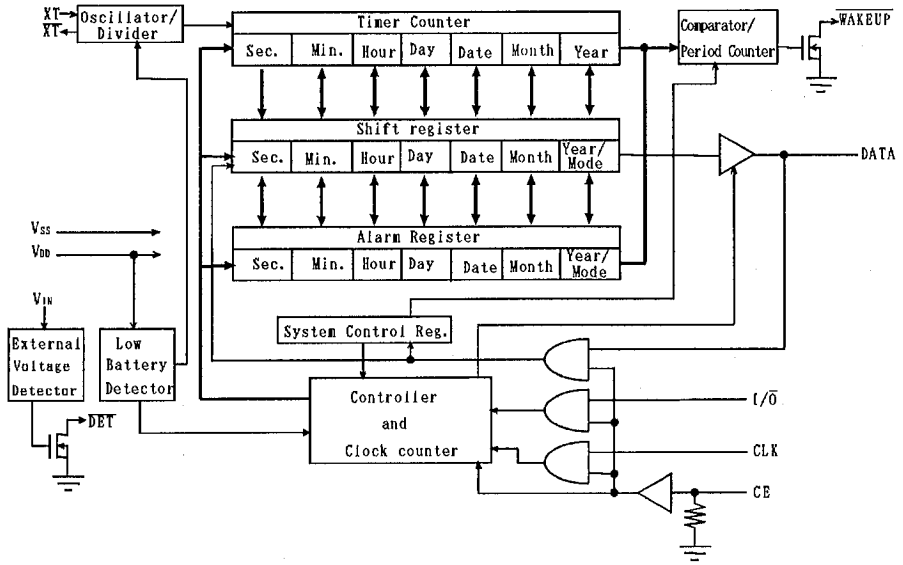
- Operating Voltage : 3.0V±20%, 5.0V±10%
  2.0 to 5.5V (The clock operation)
- Low operating current : 0.8μA (Typ.) at 2.0V
  0.8μA (Typ.) at 3.0V
  4.0μA (Typ.) at 5.0V
- BCD Counts of Seconds, Minutes, Hours, Date, Days of Week, Month and Year
- Required only 4-port for MCU interface
  (DATA, CLK, CE and I/$\overline{O}$)
- Low Battery Detect Function
- Automatic Leap Year Compensation : Up to AD 2099
- Wake-up function
- External Voltage Detector (Detecting voltage is shown below)
- Package Outline --- DIP 14/DMP 14/SSOP 14/Chip
- C-MOS Technology

■ LINE UP

External Detecting Voltage	Device Name	Package Marking	External Detecting Voltage	Device Name	Package Marking
1.8V	NJU6358X18	NJU6358AX	3.9V	NJU6358X39	NJU6358HX
1.9V	NJU6358X19	NJU6358BX	4.0V	NJU6358X40	NJU6358JX
2.0V	NJU6358X20	NJU6358CX	4.1V	NJU6358X41	NJU6358KX
2.1V	NJU6358X21	NJU6358DX	4.2V	NJU6358X42	NJU6358LX
2.2V	NJU6358X22	NJU6358EX	4.3V	NJU6358X43	NJU6358MX
2.3V	NJU6358X23	NJU6358FX	4.4V	NJU6358X44	NJU6358NX
2.4V	NJU6358X24	NJU6358GX	4.5V	NJU6358X45	NJU6358PX

Note) The "X" in the device name of the above table means the package type.
(C:CHIP, D:DIP, M:DMP, V:SSOP)

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

NO.	SYMBOL	I/O	F U N C T I O N
1 2	$\overline{XT}$ XT	INPUT OUTPUT	Quartz Crystal Connecting Terminals. (fosc=32.768kHz)
5	$\overline{DET}$	OUTPUT	External voltage detector output terminal (N-channel open-drain). "L" level is output when the voltage of VIN terminal is detected.
6	$\overline{WAKEUP}$	OUTPUT	WAKE-UP output terminal (N-channel open-drain). "L" level is output at the time of the alarm set.
7	VSS	-	GND
8	I/$\overline{O}$	INPUT	Input/Output Select Terminal for the DATA Terminal. "H": Input, "L": Output During the CE terminal is "L", the Data terminal is high impedance.
9	CE	INPUT	Chip Enable Input Terminal (with a pull-down resistor). "H" : Data Input/Output is available. "L" : Data terminal is high impedance. When the data input/output is executed consequently, the CE terminal should be set to "L" level at the data transmission interval.
10	CLK	INPUT	Clock Input Terminal. The Data Input/Output is synchronized by this clock. When the CE terminal is set to "L" level, this clock is ignored.
11	DATA	I/$\overline{O}$	Serial Data Input/Output terminal.
13	VIN	INPUT	External voltage detector input terminal.
14	VDD	-	Power Supply (+3V/+5V)
3,4,12	NC	-	No connect

I/$\overline{O}$	CE	DATA
H	H	Input
L	H	Output
*	L	High-Impedance

*:Don't Care

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■ FUNCTIONAL DESCRIPTION

1. Timer, Alarm and System control Data format

The NJU6358 has the timer function basically, and the wake-up signal can be output when the time becomes to the alarm time which is set. It can be selected at setting the alarm that how to set the alarm, which the absolute time or the period is set. And disabling the alarm is possible.

The calendar function including the last date of each month and the leap year calculation is executed automatically. The data block of the year in the timer data is the data block of the mode recognizing which consists of the bits of the mode of the wake-up output and of the wake-up period.

Only the system control data can be set instead of setting whole timer or alarm data.

The NJU6358 using BCD code which consisting of 4 bits per 1 digit. The unused bit for the timer data should be set to "0".

< Timer Data Bit Map >

	MSB							LSB	Range
System control					0	AI	A	AH	
Second	0	S6	S5	S4	S3	S2	S1	S0	0 - 59
Minute	0	m6	m5	m4	m3	m2	m1	m0	0 - 59
Hour	0	0	H5	H4	H3	H2	H1	H0	0 - 23
Days of Week					0	W2	W1	W0	1 - 7
Date	0	0	D5	D4	D3	D2	D1	D0	1 - 31
Month	0	0	0	M4	M3	M2	M1	M0	1 - 12
Year	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	0 - 99

< Alarm Data Bit Map >

	MSB							LSB	Range
System control					0	AI	A	AH	
Second	0	S6	S5	S4	S3	S2	S1	S0	0 - 59
Minute	0	m6	m5	m4	m3	m2	m1	m0	0 - 59
Hour	0	0	H5	H4	H3	H2	H1	H0	0 - 23
Days of Week					0	W2	W1	W0	1 - 7
Date	0	0	D5	D4	D3	D2	D1	D0	1 - 31
Month	0	0	0	M4	M3	M2	M1	M0	1 - 12
Mode recognizing	0	0	0	0	AS	I2	I1	I0	

< System control Data Bit Map >

System control	MSB			LSB
	0	AI	A	AH

Note) AI (Alarm Inhibit) : "0"= No Alarm "1"= Alarm output
A (Timer/Alarm Register select) : "0"= Timer register "1"= Alarm register
AH (Valid Data Number select) : "0"= Whole (Timer or Alarm) data select
"1"= System control data select only

· Mode recognizing data

AS="0": The wake-up signal is output when the timer data equalles to the alarm as shown below.
AS="1": The wake-up signal is output at the alarm period set.

AS = "0"				AS = "1"			
I_2	I_1	I_0	The valid time range	I_2	I_1	I_0	The wake-up period
0	0	0	sec.	0	0	0	1 sec.
0	0	1	min., sec.	0	0	1	2 sec.
0	1	0	hour, min., sec.	0	1	0	5 sec.
0	1	1	day, hour, min., sec.	0	1	1	10 sec.
1	0	0	date, hour, min., sec.	1	0	0	20 sec.
1	0	1	month, date, hour, min., sec.	1	0	1	30 sec.
1	1	0	same as $(I_2, I_1, I_0)=(0,0,0)$	1	1	0	60 sec.
1	1	1	same as $(I_2, I_1, I_0)=(0,0,0)$	1	1	1	same as $(I_2, I_1, I_0)=(0,0,0)$

2. Timer, Alarm and System control Data Writing

When both of the I/$\overline{O}$ terminal and the CE terminal are "H" level, the timer, alarm or system control data can be written into the shift register in the NJU6358 from the DATA terminal synchronized with the rising edge of the clock signal input from the CLK terminal.

The data type (the timer or the alarm/system control) is determinded by setting the timer/alarm register select bit (A). When the bit of the A is set to "0" (the timer data is selected), the update of the timer is stopped, the oscillator divider is cleared, and the data is transmitted from the shift register to the timer register. The oscillator divider starts operating when the CE signal is changed from "H" to "L" level. When the bit of the A is set to "1" (the alarm or system control data is selected), the counter of the second is cleared, and the data is transmitted from the shift register to the alarm register.

The input data strings are LSB first of the each digit as shown below, and the last 56-bit is effective:

< Timer Data strings >

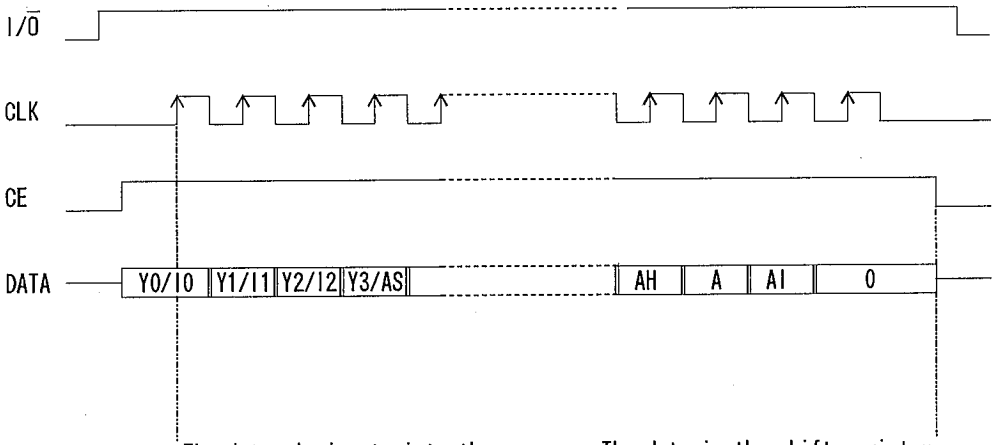
Year	Month	Date	Day	Hour	Minute	0*	System control

Note) The data of the second can not be set as the timer data.

< Alarm Data strings >

Mode recognizing	Month	Date	Day	Hour	Minute	Second	System control

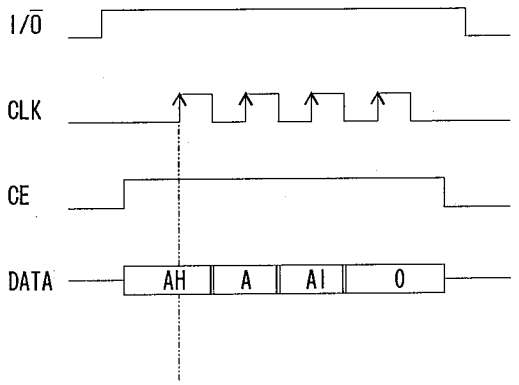
< Write-Down Timing >



The data is input into the shift register at the rising edge of the CLK signal.

The data in the shift register is transferred to the timer or alarm register at this falling edge of the CE, then the oscillator divider starts operating.

< Write-Down Timing of the system control data only >
(The condition of AH = "1")



If the AH="1" is set, the last 4-bit of the input data is only effective and written-down to the system control register.

Note) If the AH="0" is set, the last 56-bit data is effective and written-down to the timer or alarm register.

3. Timer, Alarm or System control Data Reading

When the I/O terminal is "L" level and the CE terminal is "H", the timer, alarm or system control data can be read out from the shift register in the NJU6358 through the DATA terminal synchronized with the falling edge of the clock signal input from the CLK terminal.

The data type (the timer or the alarm/system control) is determinded by setting the timer/alarm register select bit (A) before.

The timer or alarm data is transmitted from the timer register or the alarm register to the shift register when the CE terminal is set from "L" level to "H".

The input data strings are LSB first of the each digit as shown below, and the last 56-bit is effective:

Note) If the low voltage detector detect the low battery, $(EE)_H$ is written into each digit of timer data and read out. The code of $(EE)_H$ is a warning for the data broken.

Note) The difference between the read out data of timer and the actual timer data becomes 1 second in maximum, because the timer register counts up during the data is reading out.

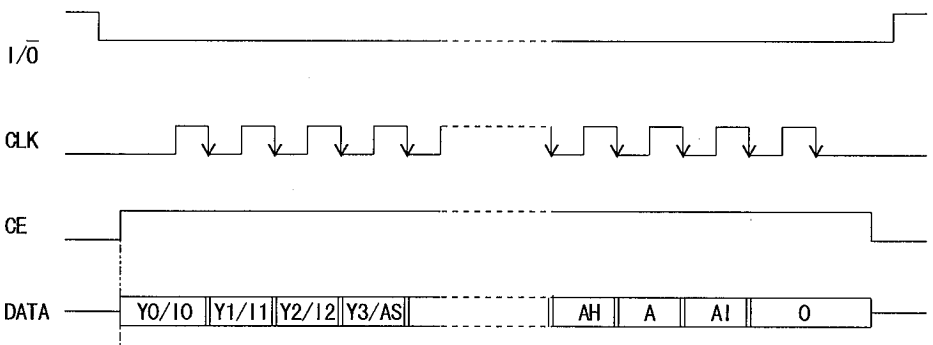
< Timer Data strings >

Year	Month	Date	Day	Hour	Minute	Second	System control

< Alarm Data strings >

Mode recognizing	Month	Date	Day	Hour	Minute	Second	System control

< Read-Out Timing >



The timer or alarm data is transferred to the shift register at the rising edge of the CE signal.

4. Voltage Detect Function

The NJU6358 series incorporate the low battery detector and the external voltage detector.

< Low battery detector >

If the supply voltage is reduced to the detection level, $(EE)_H$ is written into each digit of the shift register as the warning code for the MCU.

< External voltage detector >

If the input voltage of the V_{IN} terminal is reduced to the detection level, "L" level is output from the $\overline{DET}$ terminal. The detecting voltage which is independent of the block of the real time clock can be selected from 1.8V to 2.4V or from 3.9V to 4.5V by the step of 0.1V.

5. Data Access

The NJU6358 series can operate from 2.0V to 5.5V on the timer operating. However, it is not allow the data access out of the range of 3V±20% or 5V±10%. The data may be broken unless 3V±20% or 5V±10%.

Thus, when the data access is executed, the CE terminal should be "H" level after the power supply rises to 3V±20% or 5V±10%.

6. Data Correction

The NJU6358 series have the function of the data correction.

When the ineffective data is input, the data is corrected as show blow table. The data correction is executed for the timer data or the alarm data, however, is not executed for the system control data.

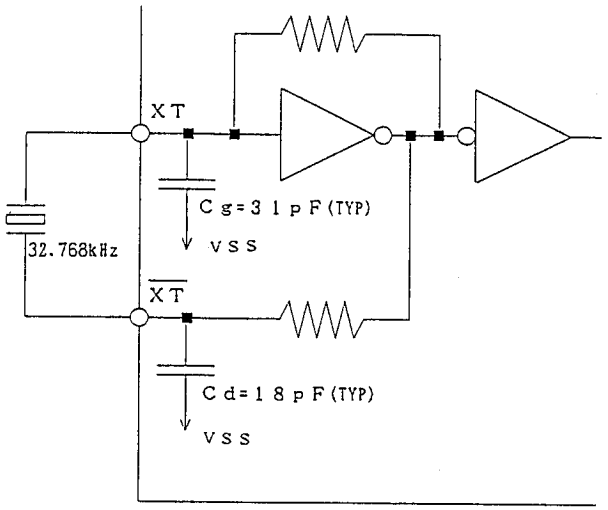
	The object data of the correction	The ineffective data	The corrected data
Second	S0 to S6	The data except 0 to 59 (Only the alarm data)	00_H
Minute	m0 to m6	The data except 0 to 59	00_H
Hour	H0 to H5	The data except 0 to 23	00_H
Day	W0 to W2	The data except 1 to 7	01_H
Date	D0 to D5	Jan., Mar., May, July, Aug., Oct., Dec. : The data except 1 to 31 Apr., June, Sep., Nov., : The data except 1 to 30 Feb. : The data except 1 to 28 Feb. in the leap year : The data except 1 to 29	01_H
Month	M0 to M4	The data except 1 to 12	01_H
Year	Y0 to Y7	The data except 0 to 99	00_H
Mode recogni-zation	I0 to I2	(I_2, I_1, I_0) = (1,1,0) at AS="0" = (1,1,1) at AS="0" = (1,1,1) at AS="1"	(0,0,0)

7. Error of Wake-up Period

When the period output mode of the wake-up is selected (AS="1"), the period error is produced as same as the wake-up period in maximum at only the first wake-up output, however, It is becomes the correct period form the second wake-up output.

8. Crystal Oscillation Circuit

The crystal oscillation circuit in the NJU6358 series incorporates the capacitor for the oscillation. Therefore, The crystal of the frequency of 32.768KHz is only required for oscillating.
However, it is required to examinate the matching of the crystal and the oscillation circuit, so that some kinds of the crystal may be required to connect the external capacitor.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	- 0.3 ~ + 6.0	V
Input Voltage of V_{IN} terminal	V_{IN}	- 0.3 ~ + 6.0	V
Input Voltage	V_I	V_{SS}-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	700 (DIP) 300 (DMP, SSOP)	mW
Operating Temperature	T_{opr}	- 30 ~ + 80	℃
Storage Temperature	T_{stg}	- 55 ~ +150	℃

NOTE 1) Decoupling capacitor should be connected between V_{DD} and V_{SS}, and between V_{IN} and V_{SS} due to the stabilized operation of the circuit.

■ ELECTRICAL CHARACTERISTICS

< Real Time Clock Block >

DC Characteristics

(V_{DD}=2.0V, V_{SS}=0V, Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	fosc=32.768kHz, No alarm, CLK=0V or V_{DD}, CE=0V			2.0	μA
Low Battery Detecting Voltage	V_{DETIN}		1.5	1.7	1.9	V

< Real Time Clock Block >

DC Characteristics 1 (V_{DD}=5.0V±10%, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage	V_{DD}		4.5		5.5	V	
Operating Current	I_{DD}	f_{OSC}=32.768kHz, No alarm, CLK=0V or V_{DD}, CE=0V		4.0	15	μA	
Input Voltage	V_{IH}	I/O, CE, CLK, DATA Terminals	V_{DD}x0.8		V_{DD}	V	
	V_{IL1}	I/O, CE, CLK, DATA Terminals	V_{SS}		V_{DD}x0.2		
Input Current	I_{CE}	CE Terminal (CE=V_{DD})			20	μA	
Input Leakage Current	I_{IL}	I/O, CLK Terminals	-1.0		1.0	μA	
Output Current	I_{OH}	DATA Terminal (V_{OH}=4.1V)	0.4			mA	
	I_{OL1}	DATA Terminal (V_{OL1}=0.4V)	1.0				
	I_{OL2}	$\overline{\text{WAKEUP}}$ Terminal (V_{OL2}=0.4V)	1.0				
Output off Leakage Current	I_{OL}	$\overline{\text{WAKEUP}}$ Terminal	-2.0		2.0	μA	
3-state Leakage Current	I_{TSL}	DATA Terminal (CE=0V)	-2.0		2.0	μA	

DC Characteristics 2 (V_{DD}=3.0V±20%, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage	V_{DD}		4.5		5.5	V	
Operating Current	I_{DD}	f_{OSC}=32.768kHz, No alarm, CLK=0V or V_{DD}, CE=0V		0.8	2.0	μA	
Input Voltage	V_{IH}	I/O, CE, CLK, DATA Terminals	V_{DD}x0.8		V_{DD}	V	
	V_{IL1}	I/O, CE, CLK, DATA Terminals	V_{SS}		V_{DD}x0.2		
Input Current	I_{CE}	CE Terminal (CE=V_{DD})			12	μA	
Input Leakage Current	I_{IL}	I/O, CLK Terminals	-1.0		1.0	μA	
Output Current	I_{OH}	DATA Terminal (V_{OH}=1.8V)	0.4			mA	
	I_{OL1}	DATA Terminal (V_{OL1}=0.4V)	1.0				
	I_{OL2}	$\overline{\text{WAKEUP}}$ Terminal (V_{OL2}=0.4V)	1.0				
Output off Leakage Current	I_{OL}	$\overline{\text{WAKEUP}}$ Terminal	-2.0		2.0	μA	
3-state Leakage Current	I_{TSL}	DATA Terminal (CE=0V)	-2.0		2.0	μA	

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< Real Time Clock Block >

AC CHARACTERISTICS 1 (V_{DD}=5.0V±10%, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
CLK Pulse "H" Period	t_{CWH}		0.47		5000	μs	
CLK Pulse "L" Period	t_{CWL}		0.47		5000	μs	
CE Set-up Time Before CLK Rising	t_{CS}		470			ns	
CE Hold Time After CLK Falling	t_{CH}		20			ns	
I/$\overline{O}$ Set-up Time Before CLK Rising	t_{DS}		60			ns	
I/$\overline{O}$ Hold Time After CLK Falling	t_{DH}		20			ns	
Write-Down Data Set-Up Time	t_{WDS}		100			ns	
Write-Down Data Hold Time	t_{WDH}		20			ns	
Data Delay Time After CLK Falling	t_{RDD}	C_L=50pF			200	ns	
$\overline{WAKEUP}$ pulse width	t_W		90	120	150	μs	2
CE pulse period	C_{EP}		200			ns	3
Rise/Fall Time	t_{RF}				50	ns	

NOTE 2) The $\overline{WAKEUP}$ terminal is pulled-up to the V_{IN} terminal connected by the 470KΩ resistor.
NOTE 3) This parameter is defined with the period of the riseing edge of the CE terminal.

AC CHARACTERISTICS 2 (V_{DD}=3.0V±20%, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
CLK Pulse "H" Period	t_{CWH}		0.47		5000	μs	
CLK Pulse "L" Period	t_{CWL}		0.47		5000	μs	
CE Set-up Time Before CLK Rising	t_{CS}		470			ns	
CE Hold Time After CLK Falling	t_{CH}		20			ns	
I/$\overline{O}$ Set-up Time Before CLK Rising	t_{DS}		60			ns	
I/$\overline{O}$ Hold Time After CLK Falling	t_{DH}		20			ns	
Write-Down Data Set-Up Time	t_{WDS}		100			ns	
Write-Down Data Hold Time	t_{WDH}		20			ns	
Data Delay Time After CLK Falling	t_{RDD}	C_L=50pF			200	ns	
$\overline{WAKEUP}$ pulse width	t_W		90	120	150	μs	4
CE pulse period	C_{EP}		200			ns	5
Rise/Fall Time	t_{RF}				50	ns	

NOTE 4) The $\overline{WAKEUP}$ terminal is pulled-up to the V_{IN} terminal connected by the 470KΩ resistor.
NOTE 5) This parameter is defined with the period of the riseing edge of the CE terminal.

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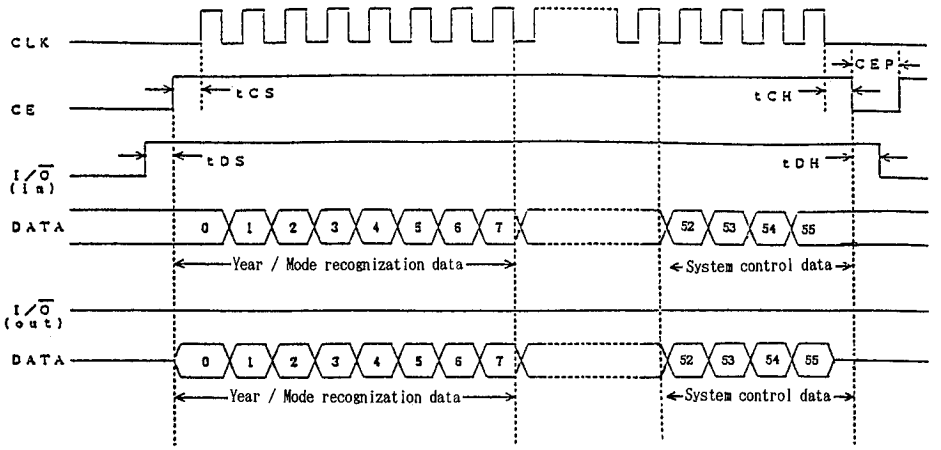
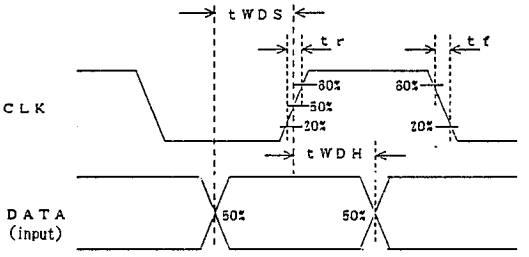
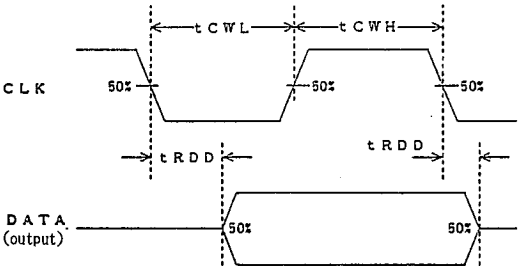
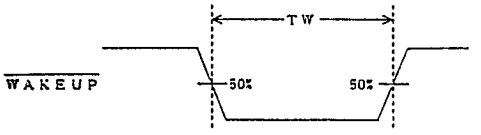
• TIMING CHART of Real Time Clock Block









< External Voltage Detector Block >

DC Characteristics (Vss=0V, Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Detecting Voltage	V_{DET}	The version of 1.8V		1.764	1.800	1.836	V	
		The version of 1.9V		1.862	1.900	1.938		
		The version of 2.0V		1.960	2.000	2.040		
		The version of 2.1V		2.058	2.100	2.142		
		The version of 2.2V		2.156	2.200	2.244		
		The version of 2.3V		2.254	2.300	2.346		
		The version of 2.4V		2.352	2.400	2.448		
		The version of 3.9V		3.822	3.900	3.978		
		The version of 4.0V		3.920	4.000	4.080		
		The version of 4.1V		4.018	4.100	4.182		
		The version of 4.2V		4.116	4.200	4.284		
		The version of 4.3V		4.214	4.300	4.386		
		The version of 4.4V		4.312	4.400	4.488		
		The version of 4.5V		4.410	4.500	4.590		
Input Current	I_{IN}	V_{IN} Terminal	V_{IN}=5V			3.6	μA	6
			V_{IN}=3V			3.0	μA	7
Output Current	I_{OLS}	$\overline{DET}$ Terminal	V_{IN}=3.7V, V_{OL}=0.4V	1.0			mA	6
			V_{IN}=1.6V, V_{OL}=0.4V	1.0			mA	7
Output off Leakage Current	I_{OL}	$\overline{DET}$ Terminal		-2.0		2.0	μA	

NOTE 6) This specification is adapted for the version of the external detecting voltage more than 3.9V.

NOTE 7) This specification is adapted for the version of the external detecting voltage less than 2.4V.

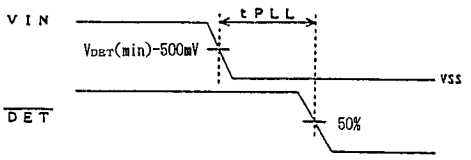
AC CHARACTERISTICS (Vss=0V, Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
$\overline{DET}$ Propagation Delay Time	t_{PLL}				100	μs	3

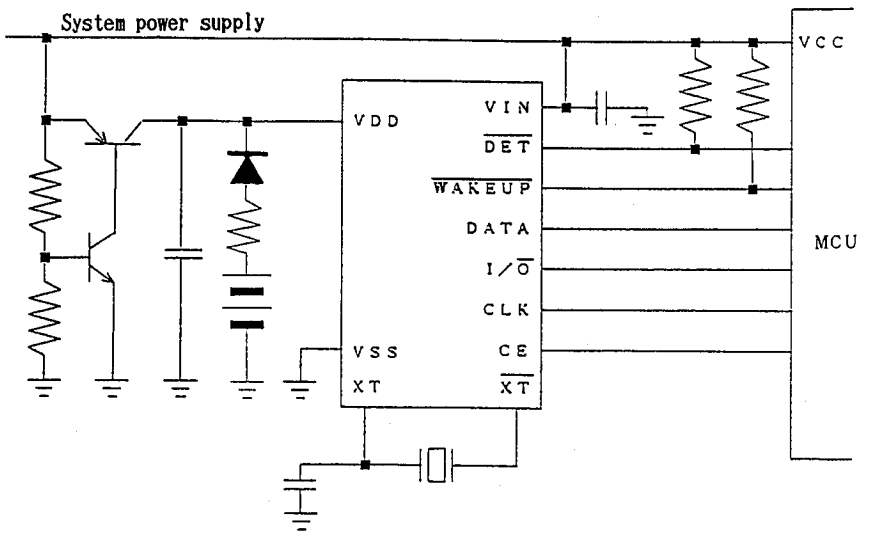
NOTE 8) This parameter is defined with the time between the falling edge of the VIN and the rising edge of the $\overline{DET}$ which terminal is pulled-up to the V_{IN} terminal connected by the 470KΩ resistor.

The condition of the falling rate of the V_{IN} is defined with 3V/100msec at the version of the external detecting voltage less than 2.4V, and is defined with 5V/100msec at the version of the external detecting voltage more than 3.9V.

• TIMING CHART of External Voltage Detector Block



■ APPLICATION CIRCUIT



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