

PCB LAYER

L1: COMPONENT
L2: GND
L3: SIGNAL1
L4: VCC
L5: SIGNAL2
L6: SIGNAL3
L7: GND
L8: COMPONENT

DC/DC&CHARGER
Switching Power
MAX1999/MAX1645

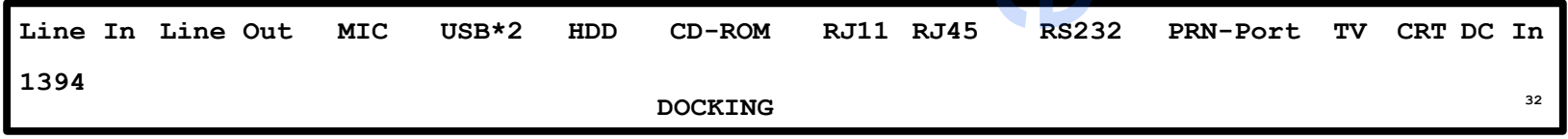
INPUTS	OUTPUTS
DCBATOUT	5V S5 3D3V_S5
	1D5V_S5 1D5V_S0 1D25V_S0 1D8V_S0 VCC_IO_S0
AD+	BT+ PAGE: 36, 41 / 39

CPU DC/DC
Switching Power
ISL6218 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 CPU_CORE_S0

OTHER DC/DC
MAX1715 37

INPUTS	OUTPUTS
DCBATOUT	1D2V_S0 2D5V_S3



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Taippei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 Document Number: J2 Rev: SD
Date: Thursday, July 17, 2003 Sheet: 1 of 42

S5

5V_S5 ○—◇— 5V_S5 14,18,26,32,36,38,42
 3D3V_S5 ○—◇— 3D3V_S5 16,17,18,25,27,31,32,34,36,38,41,42
 1D5V_S5 ○—◇— 1D5V_S5 18,41
 VCC_RTC_S5 ○—◇— VCC_RTC_S5 17

AC-IN / BAT-IN

AD+ ○—◇— AD+ 39,42
 DCBATOUT ○—◇— DCBATOUT 14,21,32,35,36,37,38,39,41,42
 DOCK_AD+ ○—◇— DOCK_AD+ 32,39
 LCD_DCBAT ○—◇— LCD_DCBAT 14
 DCBATOUT_MAX1999 ○—◇— DCBATOUT_MAX1999 36

OTHERS

5V_AUX ○—◇— 5V_AUX 27,34,36,41,42
 3D3V_AUX ○—◇— 3D3V_AUX 34,36
 UP+5V ○—◇— UP+5V 36,39,40
 BT+ ○—◇— BT+ 39,40,42
 3D3V_RTC ○—◇— 3D3V_RTC 17
 ICH_VBIAS ○—◇— ICH_VBIAS 17
 MAX1999_REF ○—◇— MAX1999_REF 36,41
 M1645_LDO_VCC ○—◇— M1645_LDO_VCC 39,40
 MAX1999_VCC ○—◇— MAX1999_VCC 36
 OP+5V ○—◇— OP+5V 26

S3

5V_S3 ○—◇— 5V_S3 31,34,37,38,39
 3D3V_S3 ○—◇— 3D3V_S3 14,25,31,32,33,38,42
 2D5V_S3 ○—◇— 2D5V_S3 7,9,10,11,37,41,42
 1D25V_DDRVREF_S3 ○—◇— 1D25V_DDRVREF_S3 7,10,37

LAN-AC

1D5V_LAN_SSAC ○—◇— 1D5V_LAN_SSAC 18,38
 3D3V_LAN_SSAC ○—◇— 3D3V_LAN_SSAC 18,19,24,38
 LAN_2D5V_SSAC ○—◇— LAN_2D5V_SSAC 23
 LAN_3D3V_SSAC ○—◇— LAN_3D3V_SSAC 23,24

CARDBUS SOCKET POWER

CB_SLOTA_VPP ○—◇— CB_SLOTA_VPP 22
 CB_SLOTA_VCC ○—◇— CB_SLOTA_VCC 22
 CB_SLOTB_VPP ○—◇— CB_SLOTB_VPP 22
 CB_SLOTB_VCC ○—◇— CB_SLOTB_VCC 21,22

S0

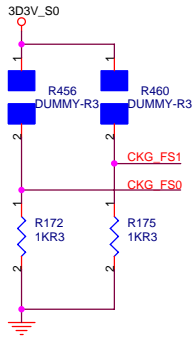
5V_S0 ○—◇— 5V_S0 13,14,17,18,19,22,25,26,27,28,29,30,31,33,34,35,38,41,42
 3D3V_S0 ○—◇— 3D3V_S0 3,4,5,7,8,9,10,13,14,15,16,17,18,19,20,21,22,23,25,27,28,29,30,31,33,34,35,38,41,42
 1D8V_S0 ○—◇— 1D8V_S0 21,41
 1D5V_S0 ○—◇— 1D5V_S0 8,9,13,15,16,18,30,41
 1D25V_S0 ○—◇— 1D25V_S0 11,12,41
 1D2V_S0 ○—◇— 1D2V_S0 7,9,37,41
 VCC_CORE_S0 ○—◇— VCC_CORE_S0 6,35
 VCC_IO_S0 ○—◇— VCC_IO_S0 4,5,6,7,9,17,18,35,41
 1D8V_VCCA_S0 ○—◇— 1D8V_VCCA_S0 5
 5V_G768_S0 ○—◇— 5V_G768_S0 34
 5VA_S0 ○—◇— 5VA_S0 25,26,42
 AUD_VREF_S0 ○—◇— AUD_VREF_S0 26
 3D3V_LCD_S0 ○—◇— 3D3V_LCD_S0 14
 CRT_VCC_S0 ○—◇— CRT_VCC_S0 13

→ **AUDIO**
 → **LCD**
 → **CRT**

5V_MOD_5VAD_S0 ○—◇— 5V_MOD_5VAD_S0 19
 3D3V_MODRSMVCC_S0 ○—◇— 3D3V_MODRSMVCC_S0 19
 TV3D3V1_S0 ○—◇— TV3D3V1_S0 15
 TV3D3VA_S0 ○—◇— TV3D3VA_S0 15
 TV3D3V2_S0 ○—◇— TV3D3V2_S0 15
 TV1D5V_S0 ○—◇— TV1D5V_S0 15

→ **MINI PCI**
 → **TV-OUT**

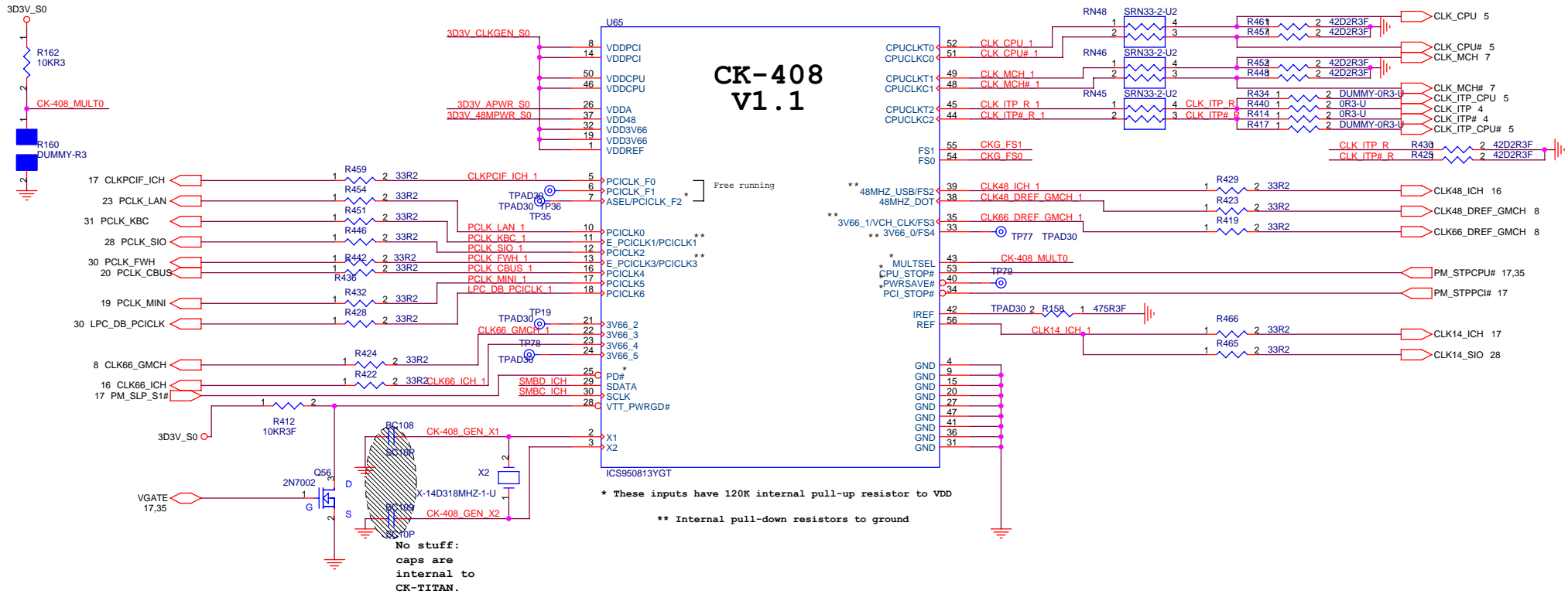
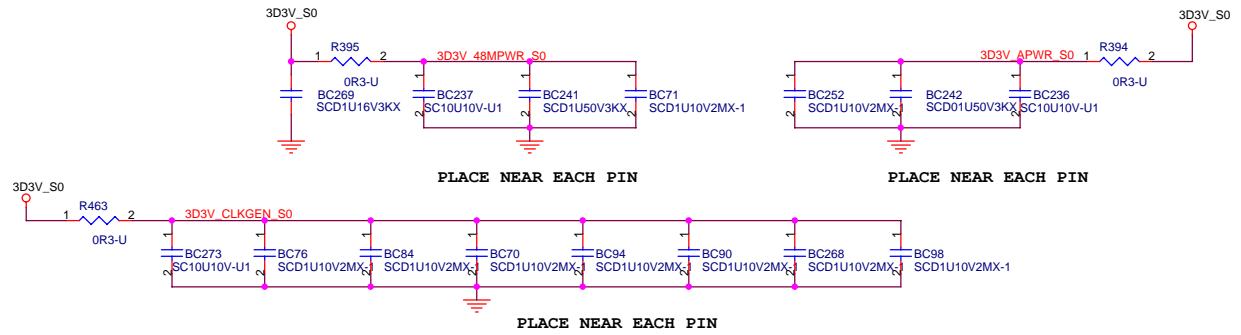
CPU & MEMORY Freq. Selection



Frequency Setting			
CPU	AGP	PCI	
FS1/0 = 00	100.00MHz	66.67MHz	33.33MHz
FS1/0 = 01	133.33MHz	66.67MHz	33.33MHz
FS1/0 = 10	200.00MHz	66.67MHz	33.33MHz
FS1/0 = 11	166.66MHz	66.67MHz	33.33MHz

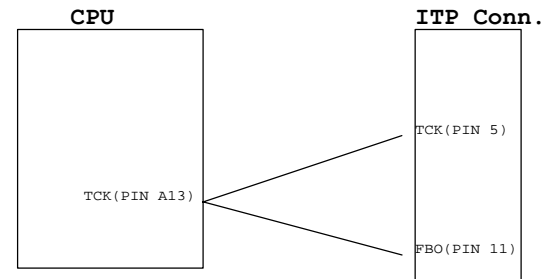
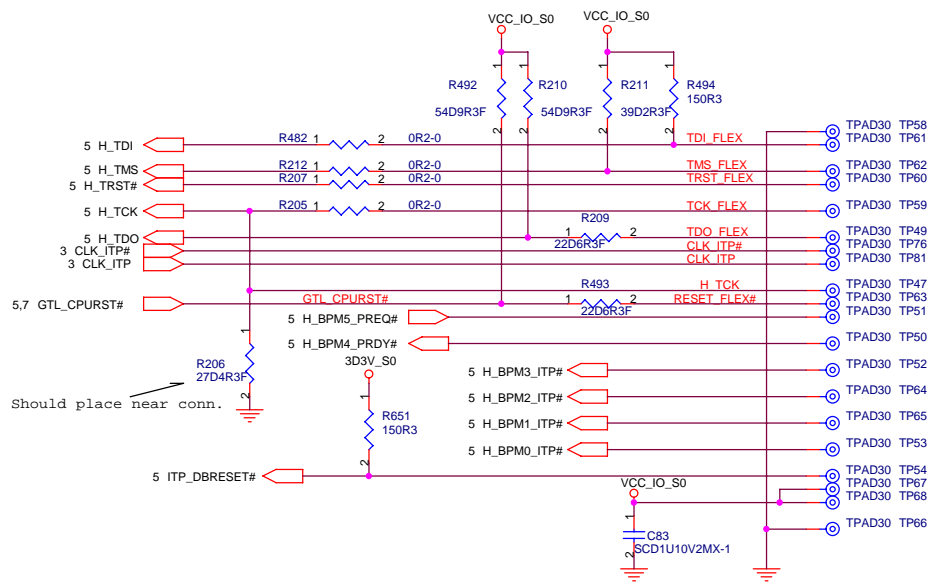
FS2 = 0 unbuffer mode (disable 66MHz-IN)
FS2 = 1 buffer mode

Mult0 = 0 Rr=221,Iref=5mA
 =>Vswing=1.0V@50ohm
Mult0 = 1 Rr=475,Iref=2.32mA
 =>Vswing=0.7V@50ohm



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Title	
Clock GEN.	
Size	Document Number
A3	J2
Date:	Rev
Thursday, July 17, 2003	SD
Sheet	of
3	42

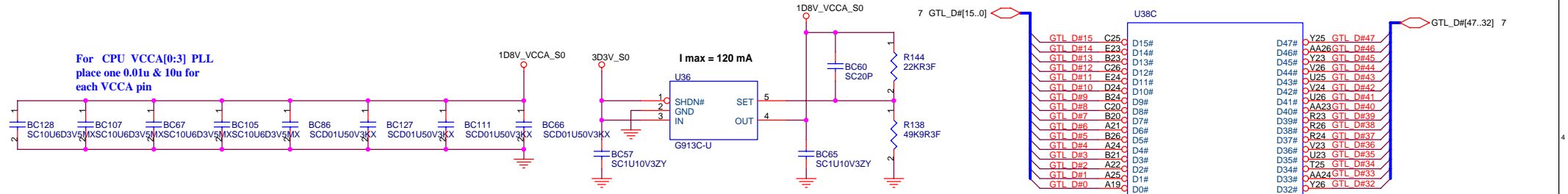
ITP Debug Pad



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Title		
ITP		
Size	Document Number	Rev
A3	J2	SD
Date:	Thursday, July 17, 2003	Sheet 4 of 42

For CPU VCCA[0:3] PLL
place one 0.01u & 10u for
each VCCA pin



Layout note:
COMP0 and COMP2 need to
be Zo=27.4ohm traces.
COMP1 and COMP3 should be
routed as Zo=55ohm,
traces shorter than 0.5".

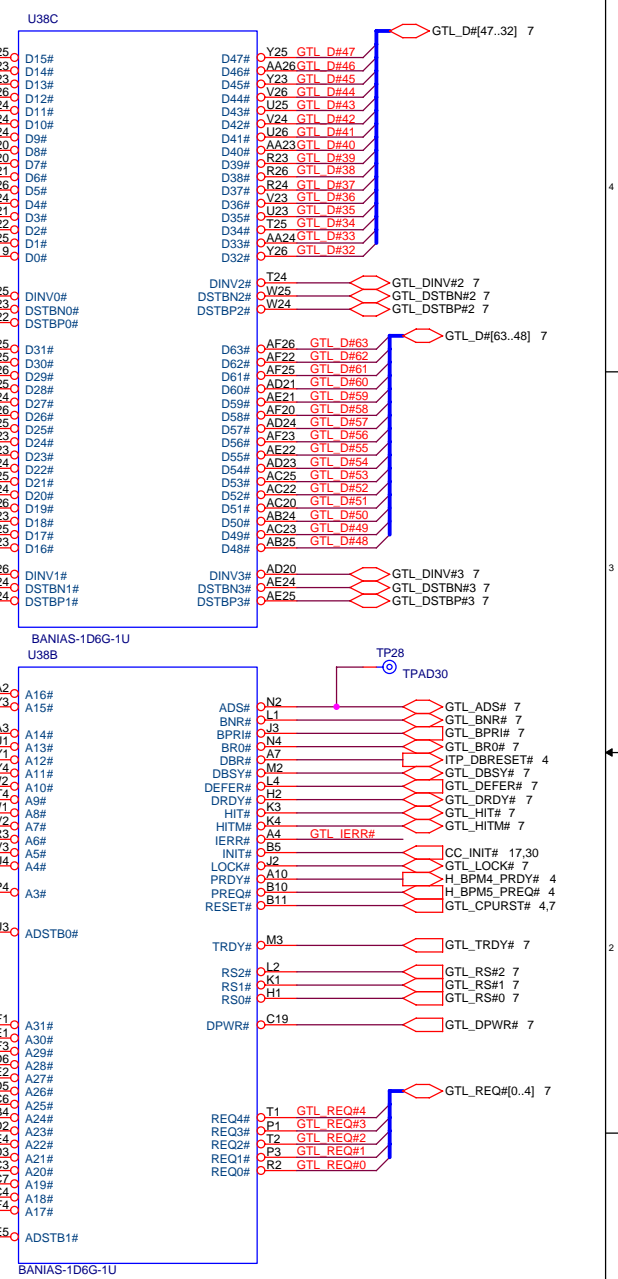
Voltage divider placed
within 0.5" of CPU pin
via a Zo=55ohm trace.

A1 stepping: No stuff
A0 stepping: stuff
R213, R176

place within 2" to CPU

Place these two
resistors near pin
AE7, AF6

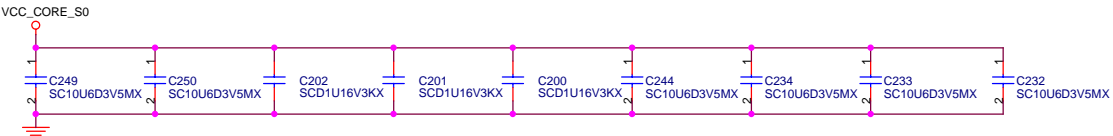
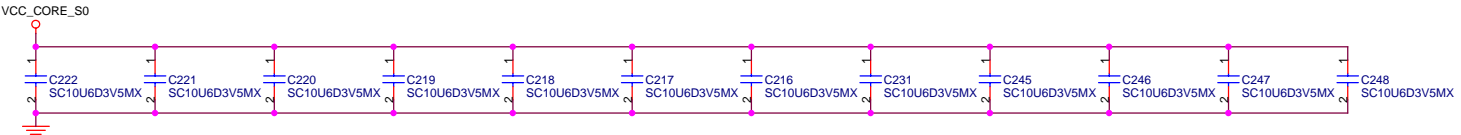
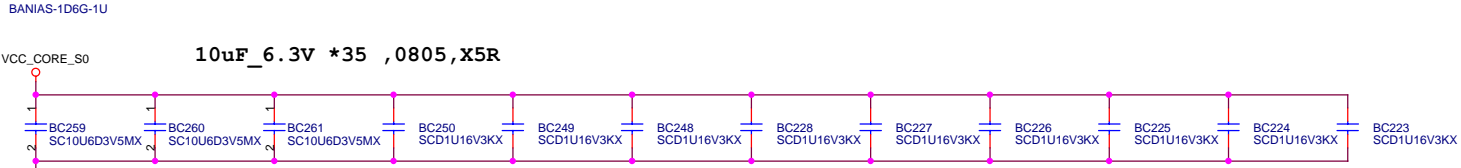
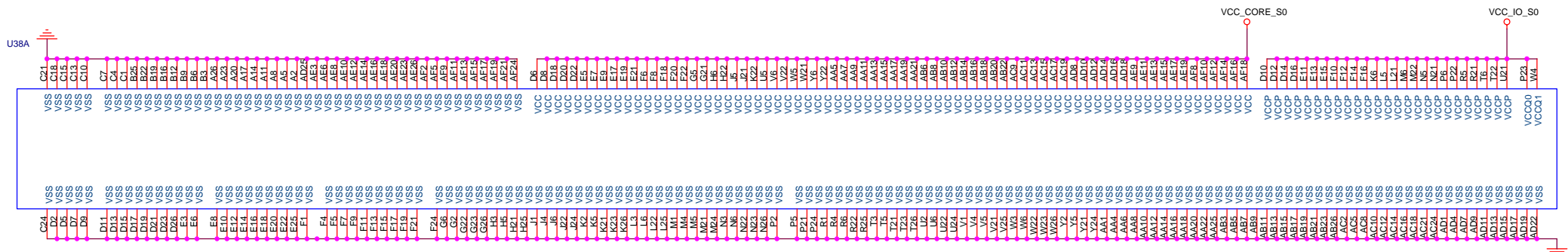
change to *71.BANIA.L02*1.3G



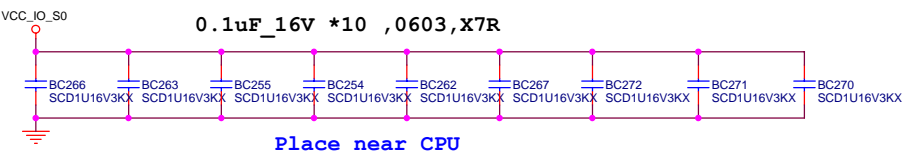
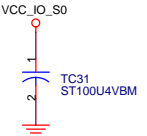
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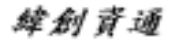
Title		
Banias CPU (1 of 2)		
Size	Document Number	Rev
A3	J2	SD
Date:	Thursday, July 17, 2003	Sheet 5 of 42

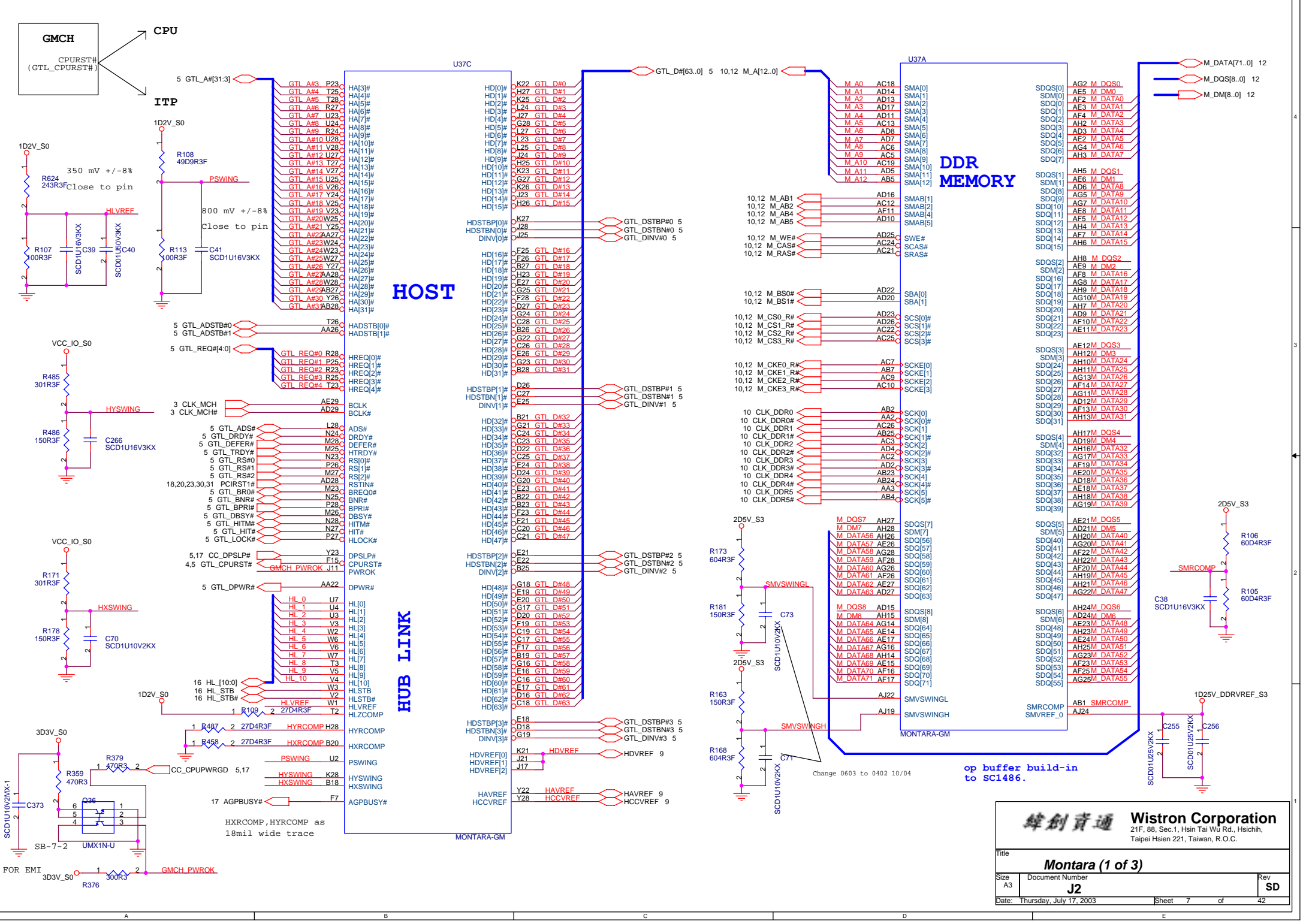
Ref 10598 EMTS
P69 need place
Decoupling
near between
VCCQ ???



Change them (C18,C17,C16,BC40,BC39,BC38,BC37,BC36,BC35,BC34,BC33,BC32)
from 10u to 1u

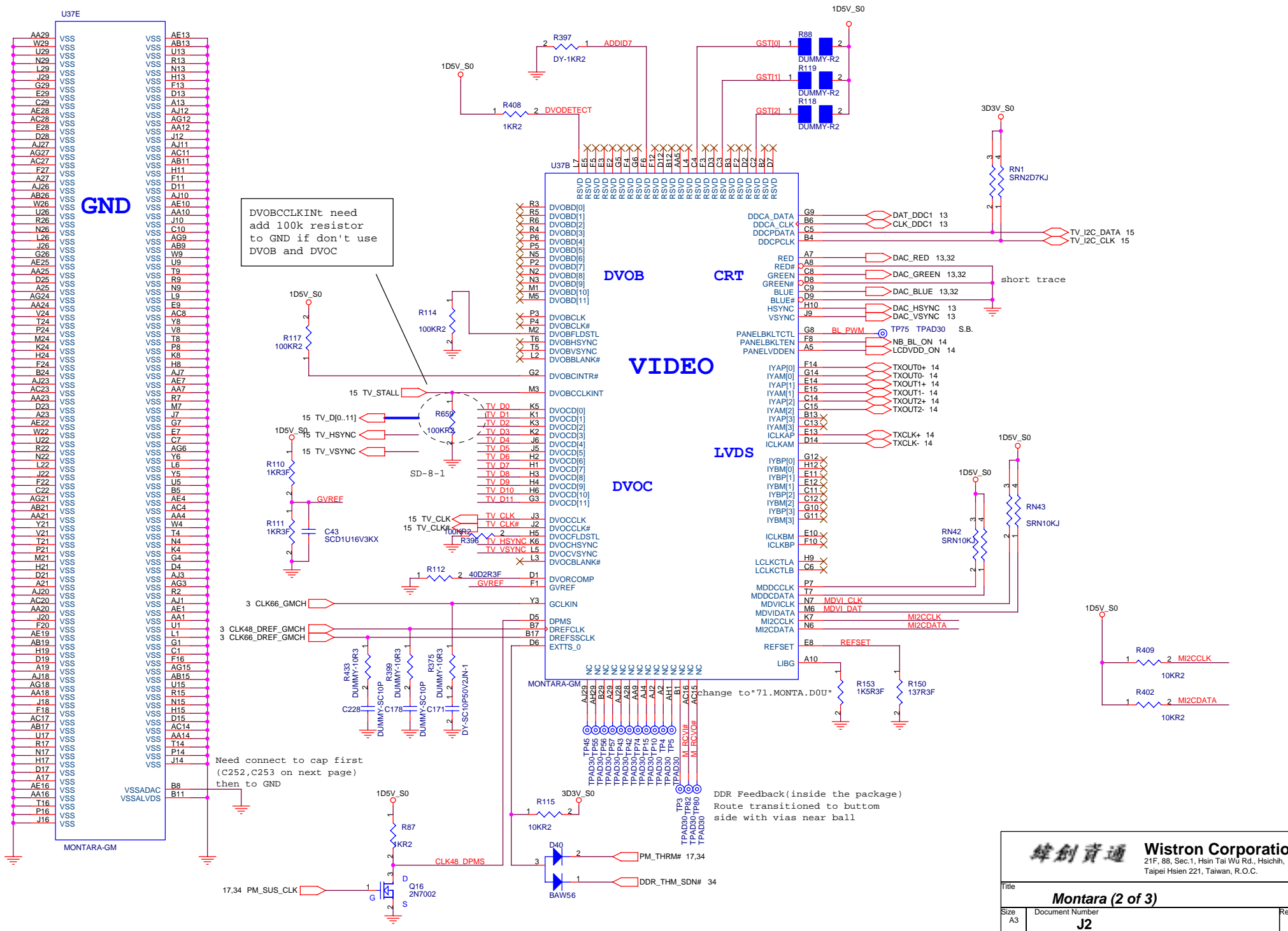


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Title	
Banias CPU (2 of 2)	
Size A3	Document Number J2
Date: Thursday, July 17, 2003	Rev SD
Sheet 6	of 42

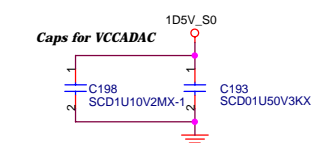
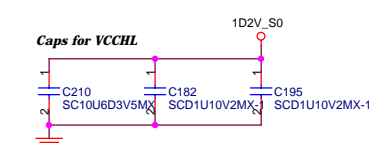
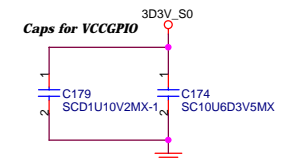
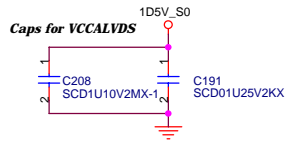
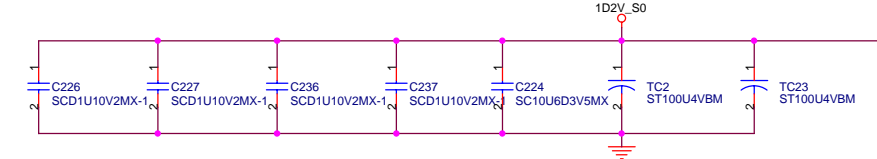
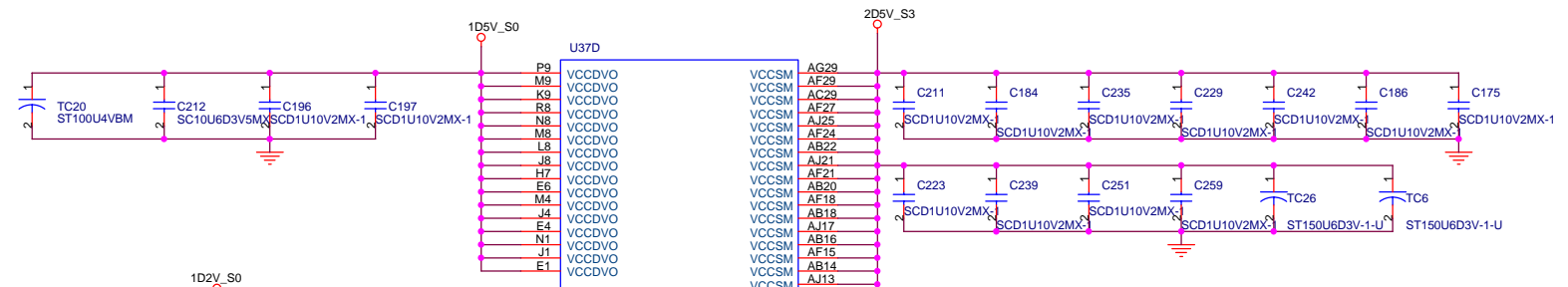


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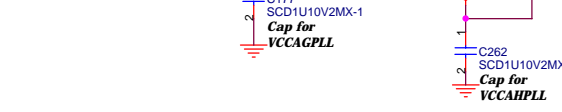
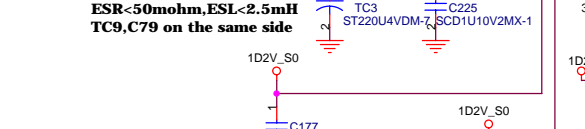
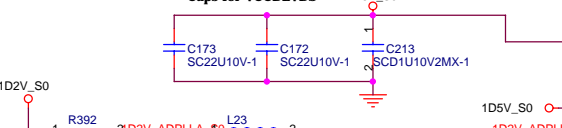
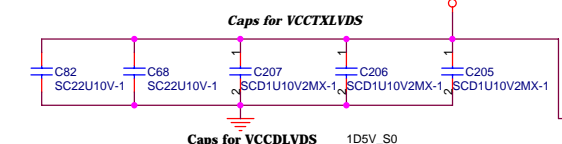
Title		
Montara (1 of 3)		
Size	Document Number	Rev
A3	J2	SD
Date: Thursday, July 17, 2003	Sheet 7 of 42	



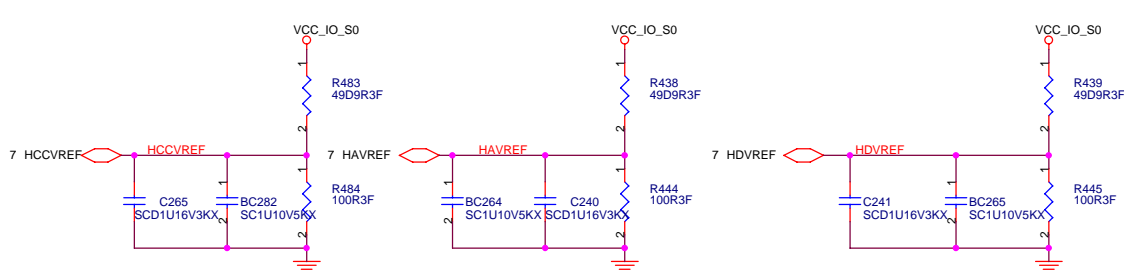
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Title	
Montara (2 of 3)	
Size A3	Document Number
	J2
Date: Thursday, July 17, 2003	Rev SD
Sheet 8	of 42



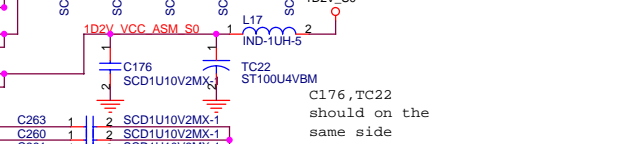
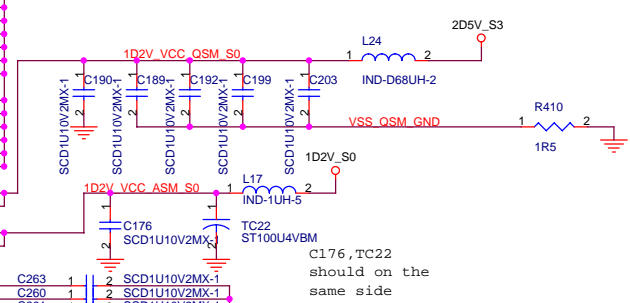
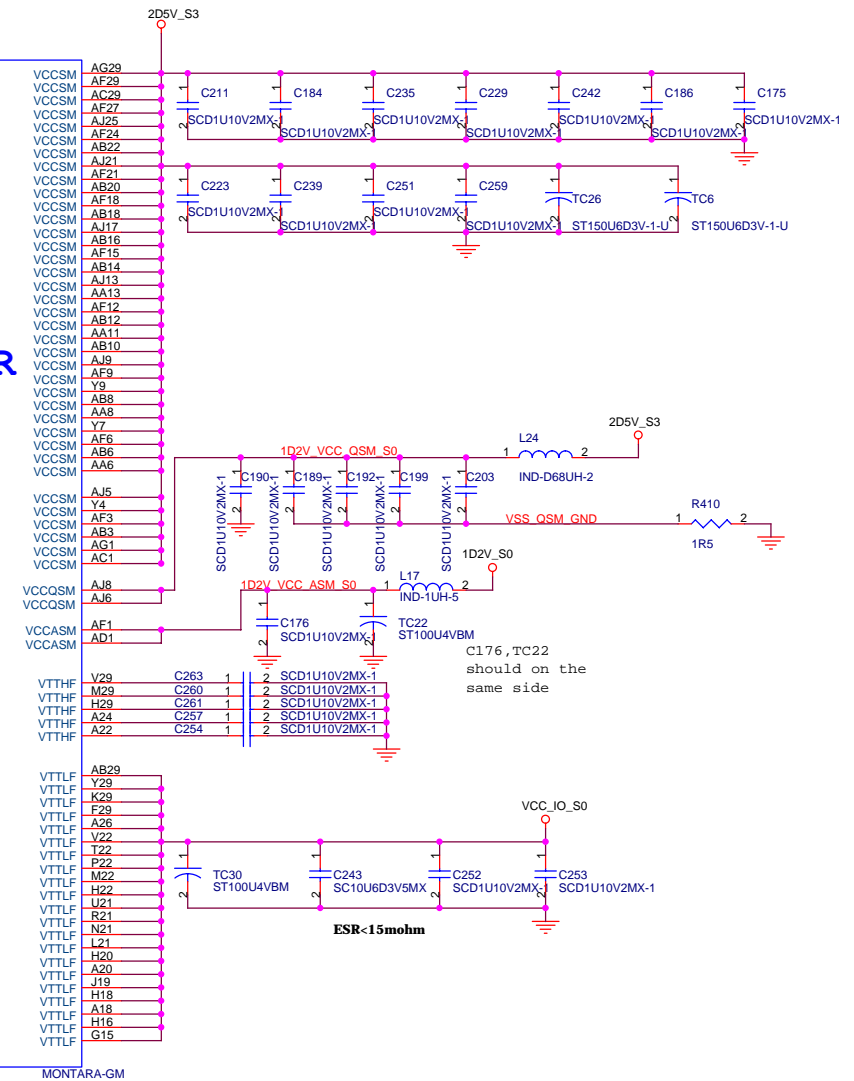
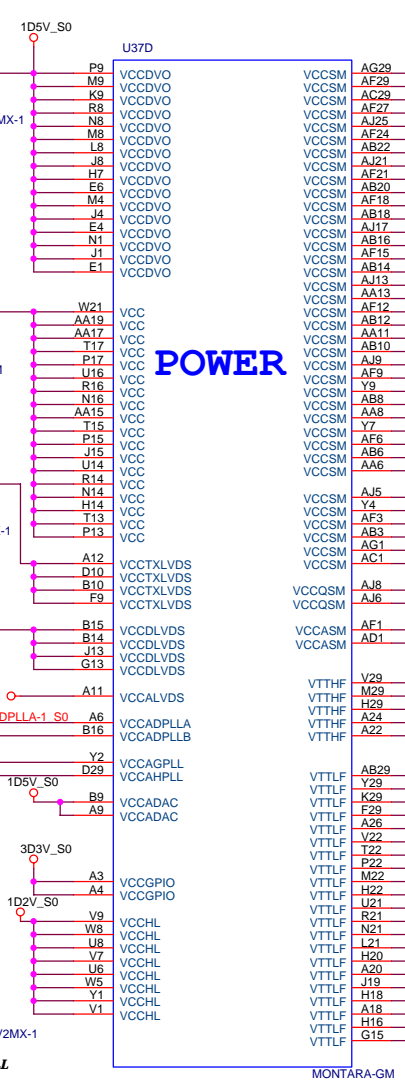
This two cap should connect to VSSADAC first then to GND



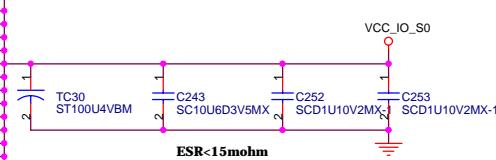
Reference Voltage: 2/3 Vcc_IO_S0



POWER

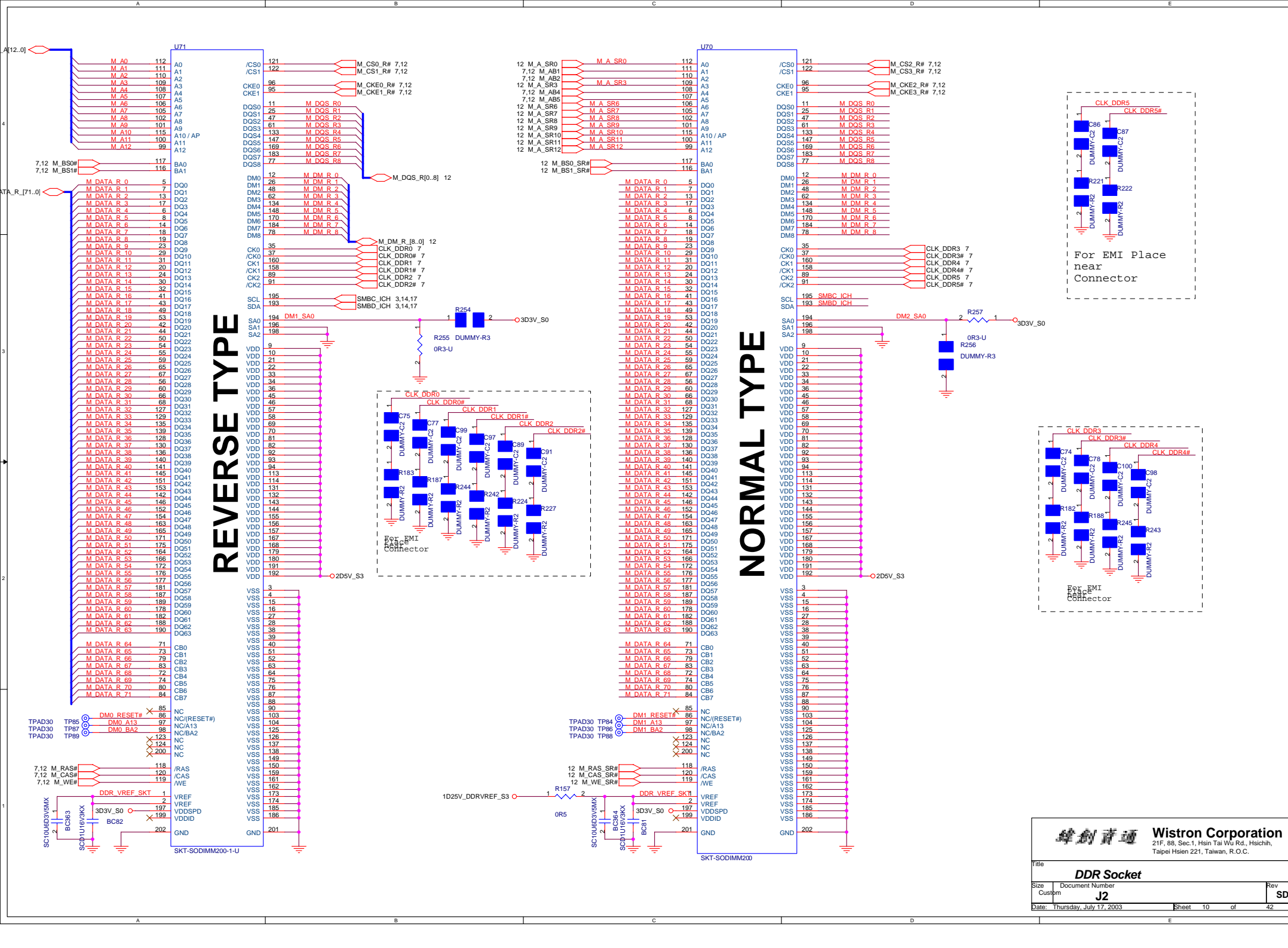


C176, TC22 should on the same side



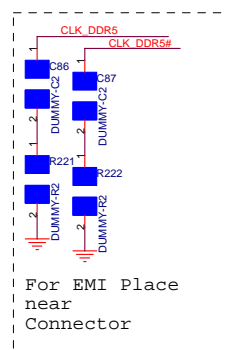
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Title		Montara (3 of 3)	
Size	Document Number	Rev	
A3	J2	SD	
Date:	Thursday, July 17, 2003	Sheet	9 of 42

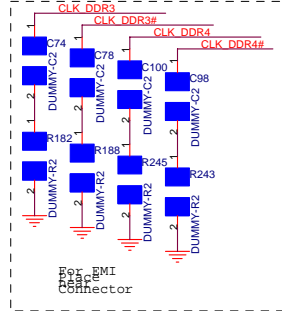


REVERSE TYPE

NORMAL TYPE



For EMI Place near Connector



For EMI Place near Connector

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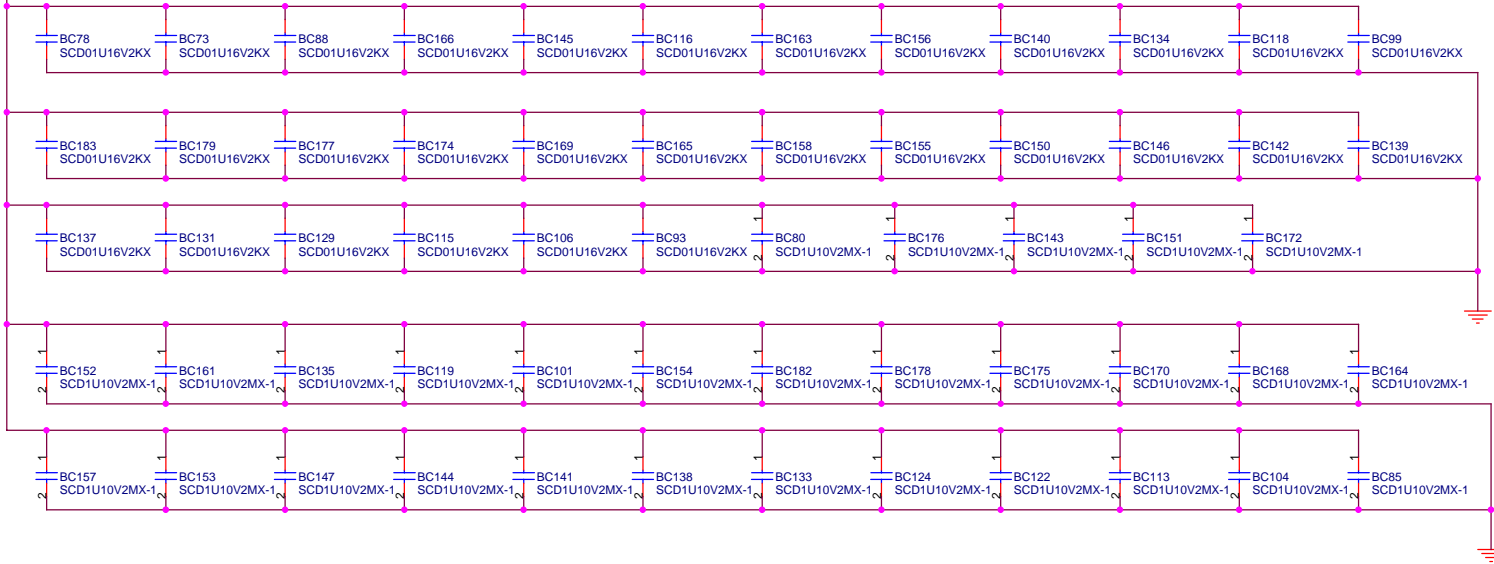
Title: **DDR Socket**

Size: Custom | Document Number: **J2** | Rev: **SD**

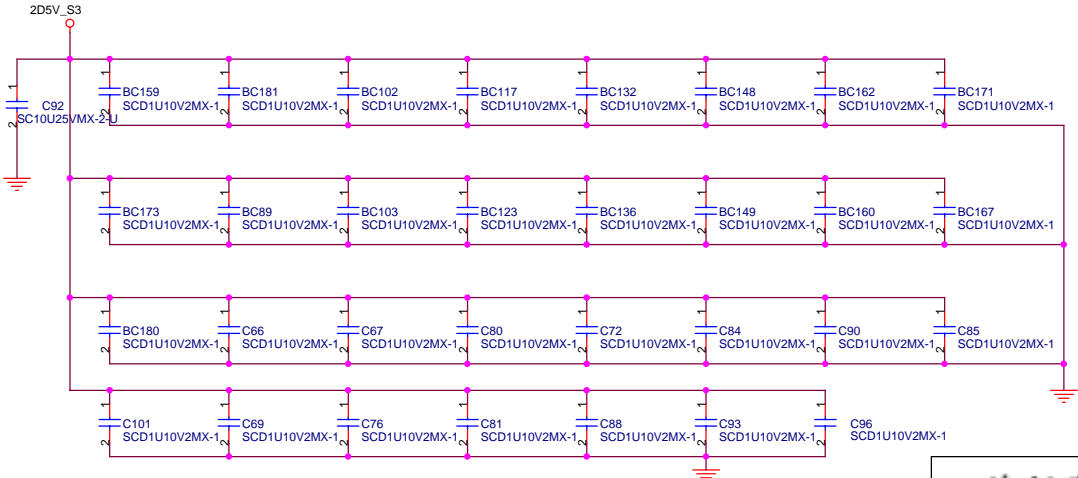
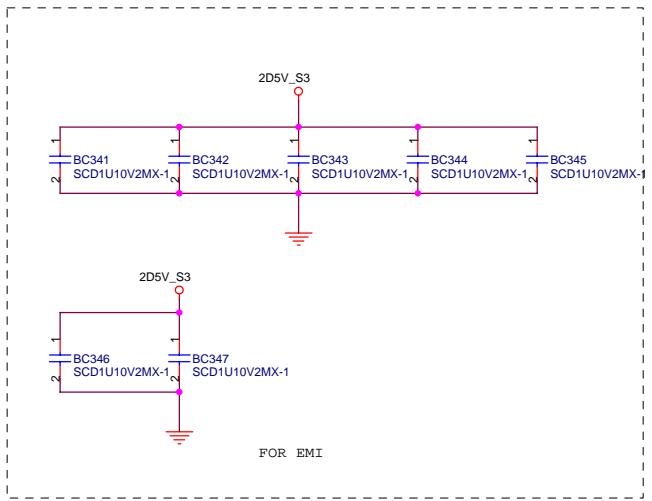
Date: Thursday, July 17, 2003 | Sheet: 10 of 42

1D25V_S0

PLACE ONE 0.1 and ONE 0.01 CAP CLOSE TO EVERY 4
PULL-UP TERMINATION RESISTORS, CRB-P13
DATA(64)+ADD(13)+DQS(9)+CB(8)+CMD(13)=107
0.1UF 0402 X7R 59X

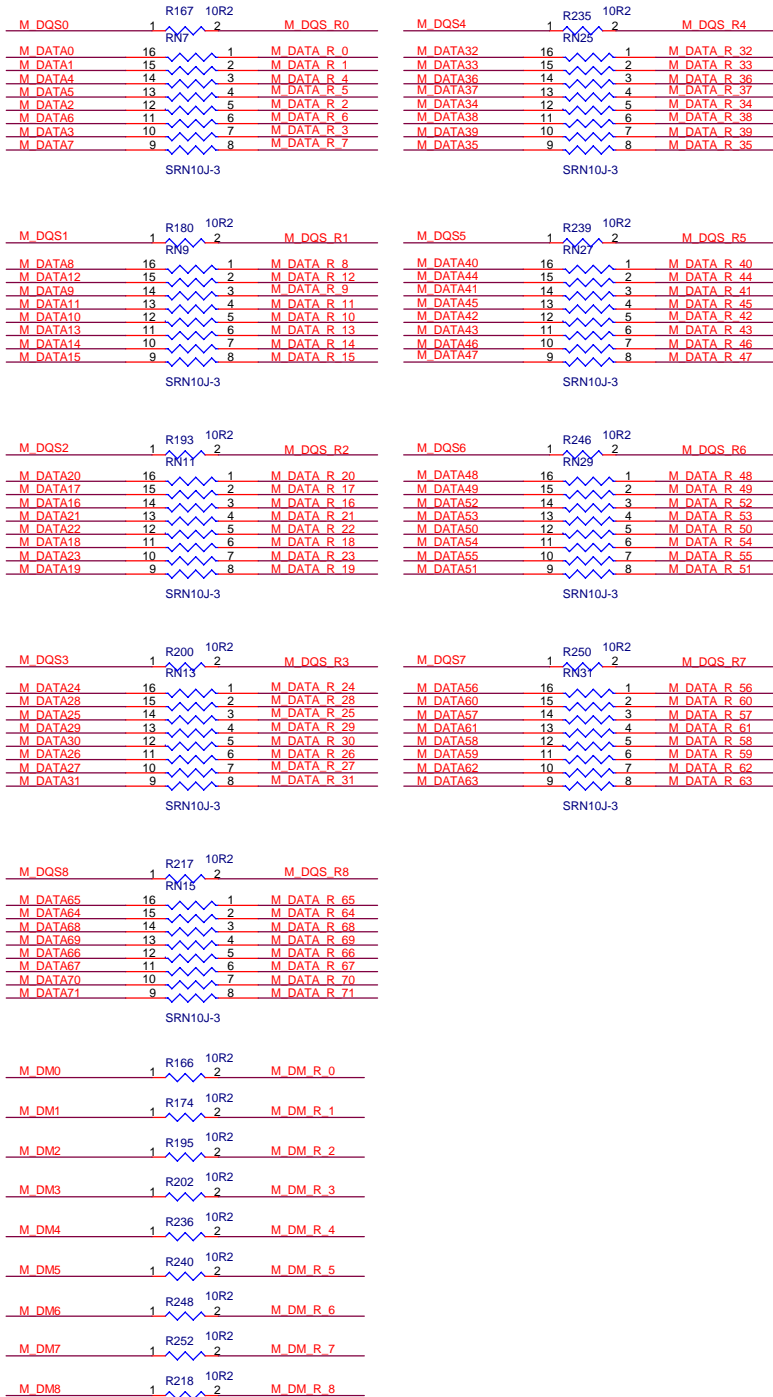


PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER
PIN

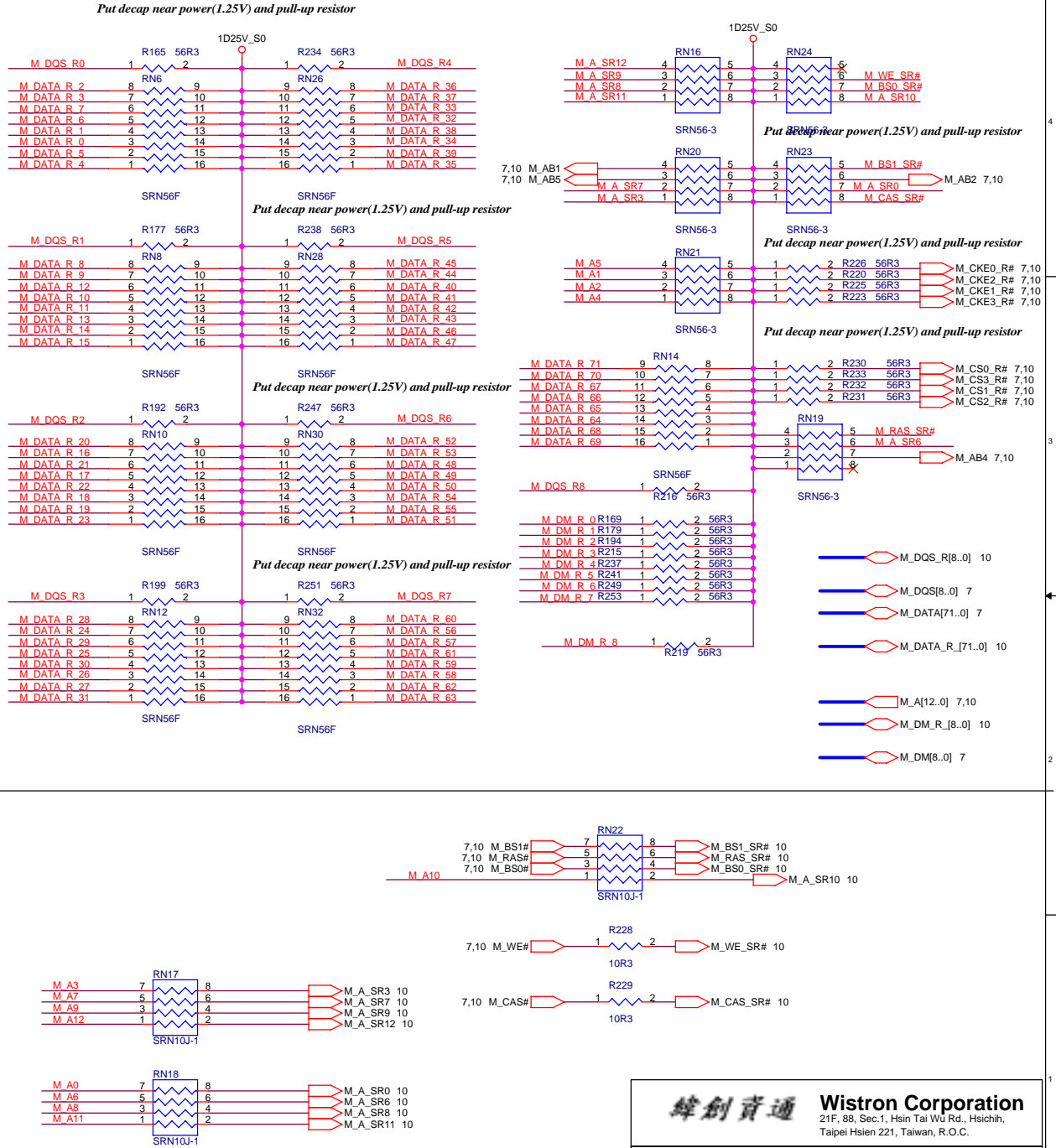


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Title	
DDR Decoupling CPA	
Size	Document Number
A3	J2
Date:	Rev
Thursday, July 17, 2003	SD
Sheet	of
11	42

SERIES DAMPING



PARALLEL TERMINATION



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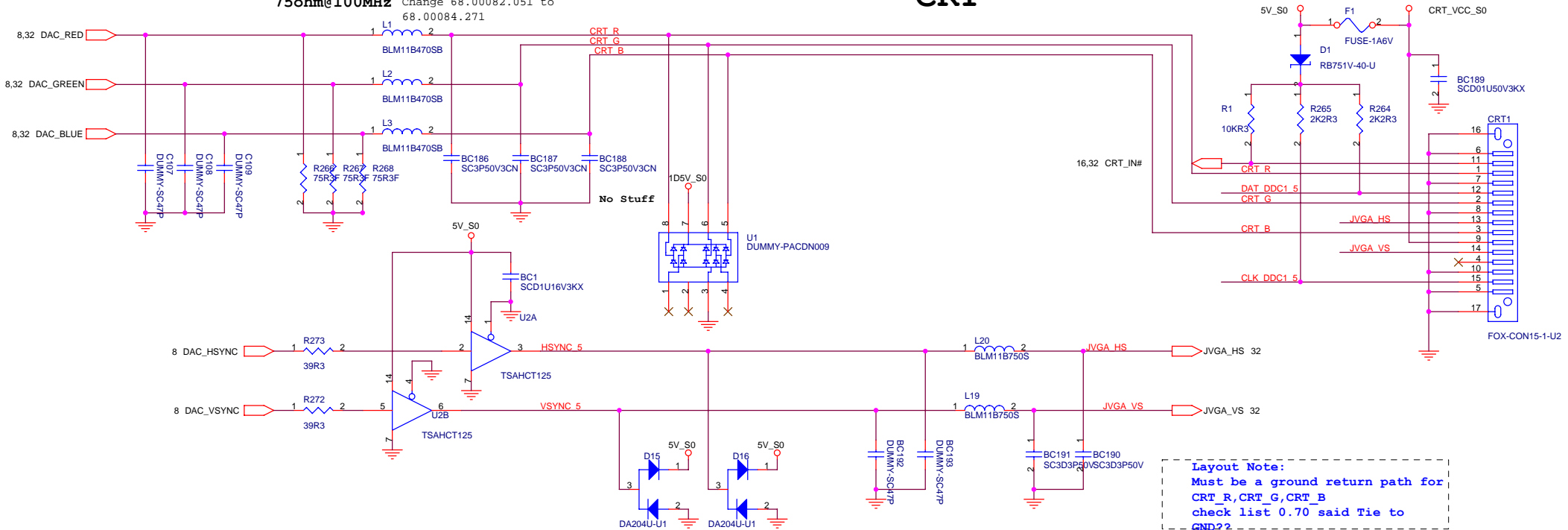
Title: **DDR Serial/Terminator Resistor**

Size: A3 Document Number: **J2** Rev: **SD**

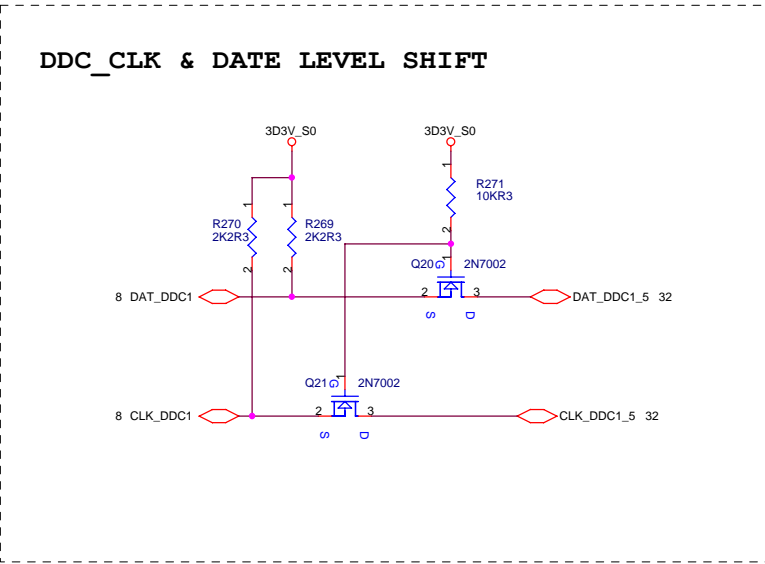
Date: Monday, August 11, 2003 Sheet 12 of 42

Ferrite bead impedance:
75ohm@100MHz
 Change 68.00082.051 to
 68.00084.271

CRT

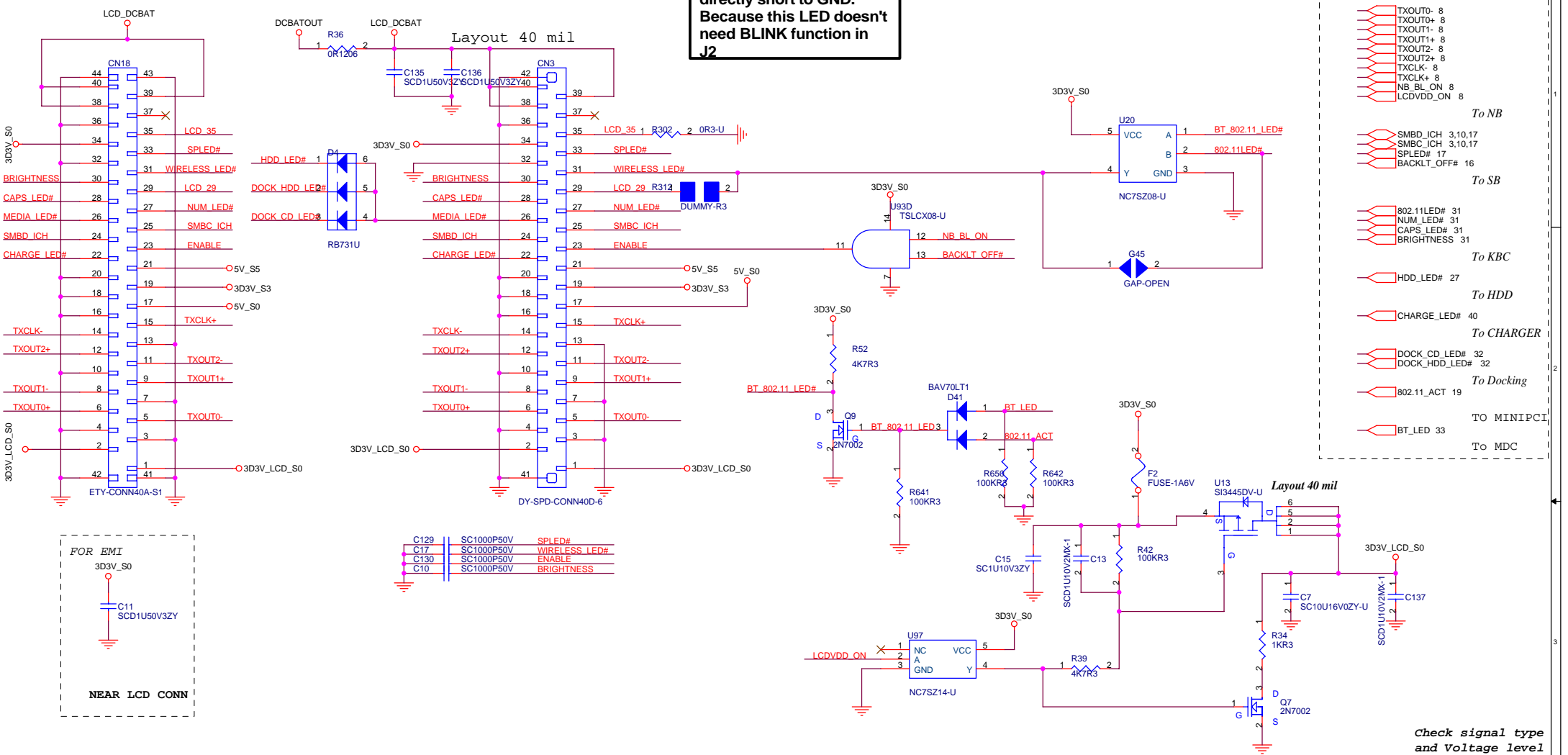


Layout Note:
 Must be a ground return path for
 CRT R, CRT G, CRT B
 check list 0.70 said Tie to
 GND??

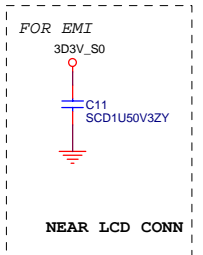


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Title	
CRT CONN.	
Size	Document Number
A3	J2
Date:	Rev
Thursday, July 17, 2003	SD
Sheet	of
13	42

Pin 32 "PWR_LED#" is directly short to GND. Because this LED doesn't need BLINK function in J2



- LVDS I/F**
- TXOUT0- 8
 - TXOUT0+ 8
 - TXOUT1- 8
 - TXOUT1+ 8
 - TXOUT2- 8
 - TXOUT2+ 8
 - TXCLK- 8
 - TXCLK+ 8
 - NB_BL_ON 8
 - LCDVDD_ON 8
- To NB
- SMBC_ICH 3,10,17
 - SMBC_ICH 3,10,17
 - SPLD# 17
 - BACKLT_OFF# 16
- To SB
- 802.11LED# 31
 - NUM_LED# 31
 - CAPS_LED# 31
 - BRIGHTNESS 31
- To KBC
- HDD_LED# 27
- To HDD
- CHARGE_LED# 40
- To CHARGER
- DOCK_CD_LED# 32
 - DOCK_HDD_LED# 32
- To Docking
- BT_LED 33
- To MINIPCI
- To MDC



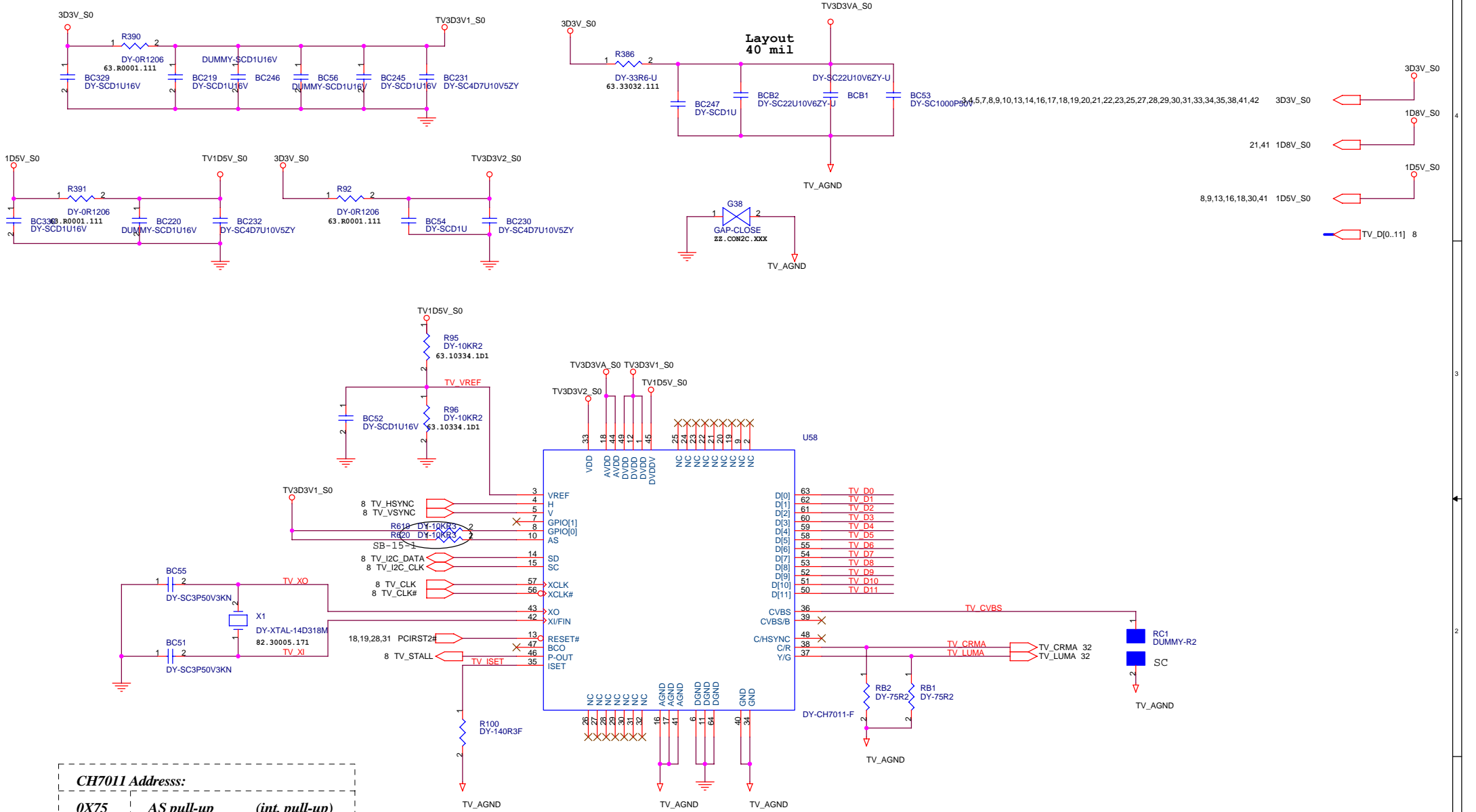
Power Plane	S5	S5	S5	S0	S5	S5	S5	S5		
Control Signal	PM_SLP_S5#	PM_SLP_S3#	PM_SLP_S1#	EMAIL_LED	STDBYLED_EN#	SPLD	STDBYLED#	Standby_LED	E_mail_LED	
POWER ON DFAULT	H	H	H	L	H	FLASH	L	OFF	OFF	
S0 without E_mail LED	H	H	H	L	H	Flash	L	OFF	OFF	
S0 with E_mail LED	H	H	H	H	H	Flash	L	OFF	Flash	
S1 without E_mail LED	H	H	L	L	L	L	L	ON	OFF	
S3	H	L	L	L	L	L	L	ON	OFF	
Enter/Leave S4 without E_mail LED	H	L	L	L	L	Flash	FLASH	Flash	OFF	
Enter/Leave S4 with E_mail LED	H	L	L	H	L	Flash	FLASH	Flash	OFF	
S4/S5	H	L	L	L	H	FLASH	L	OFF	OFF	

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Title: **LCD CONN & INVERTER**

Size A3 Document Number **J2** Rev **SD**

Date: Wednesday, August 27, 2003 Sheet 14 of 42



CH7011 Address:

0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

Power up default:

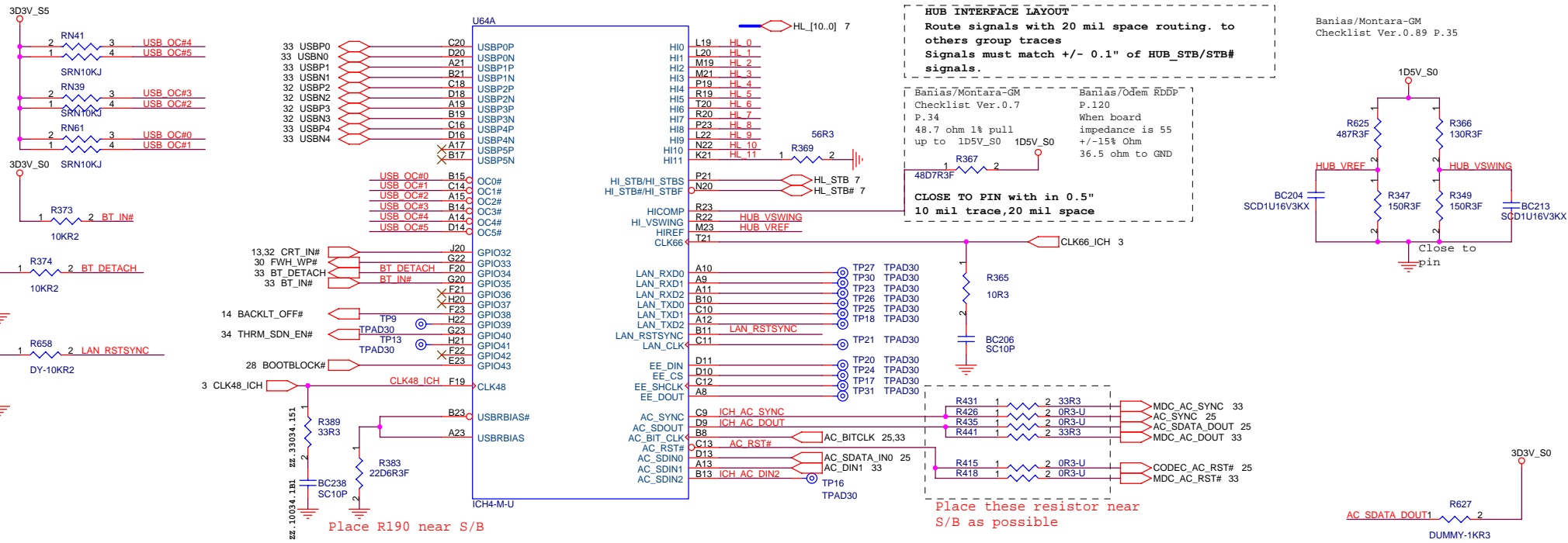
NTSC	GPI00 pull-up	(int. pull-up)
PAL	GPI00 pull-down	

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Title: **TV ENCODER**

Size A3	Document Number	Rev SD
	J2	

Date: Thursday, July 17, 2003 Sheet 15 of 42



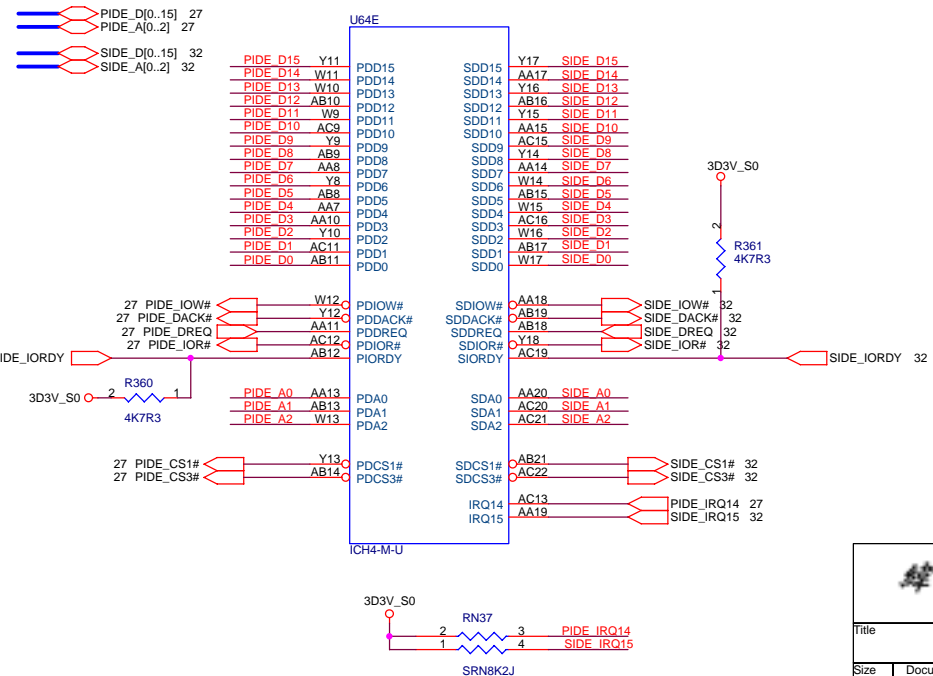
ICH4 Integrated Pull-up and Pull-down Resistors

ICH4 EDS 11450 1.1

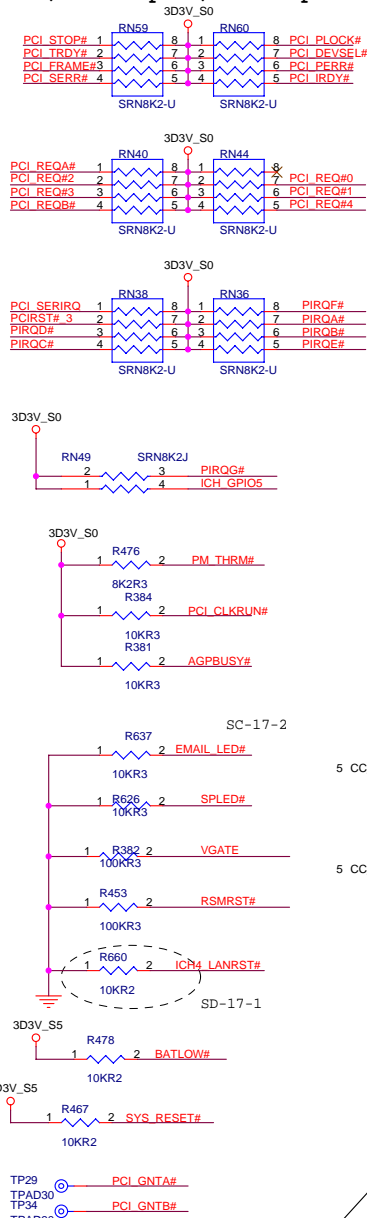
EE_DIN, EE_DOUT, PME#, FWRBTN# GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	ICH4 internal 20K pull-ups
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

ICH4 IDE Integrated Series Termination Resistors

PDD[15:0], SDD[15:0], PDIOW#, SDIOW#, PDIOR#, PDIOIOW#, PDREQ, SDREQ, PDDACK#, SDDACK#, PIORDY, SIORDY, PDA[2:0], SDA[2:0], PDCS1#, SDCS1#, PDCS3#, SDCS3#, IRQ14, IRQ15,	approximately 33 ohm
---	----------------------



PCI/Interrupt I/F Pullups



REQ4:RealTek LAN
REQ0:Mini PCI
REQ1:R5C590

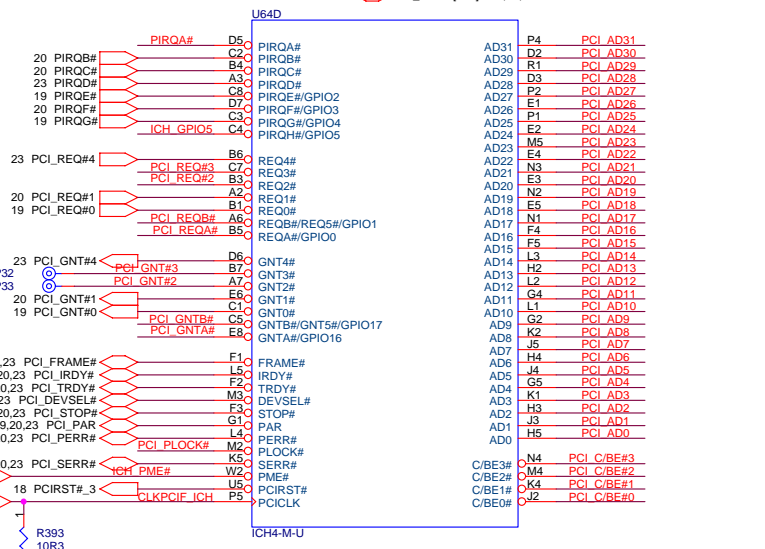
ICH_PME#
Internal Pull-up

VCC_RTC_S5

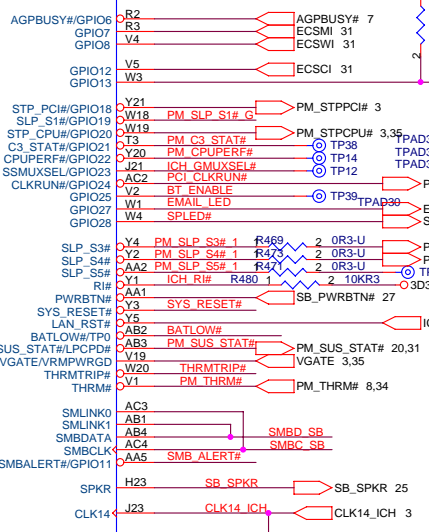
Should go high no sooner than 10mS after both +3VUN and +1.8VRUN have reach their nominal voltage
Should go high no sooner than 10mS after both +3VUS and +1.8VUS have reach their nominal voltage

If ICH-4 LAN not used, 10K ohm pd or connect directly to ---RSMRST# (SUSPWROK)
But in Bon connect to PWROK (DELAY_IMVP_PWRGD)

PCI_AD[31..0] 19,20,23
PCI_C/BE#[3..0] 19,20,23

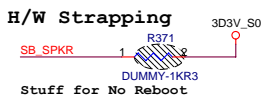


BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSP# instead)

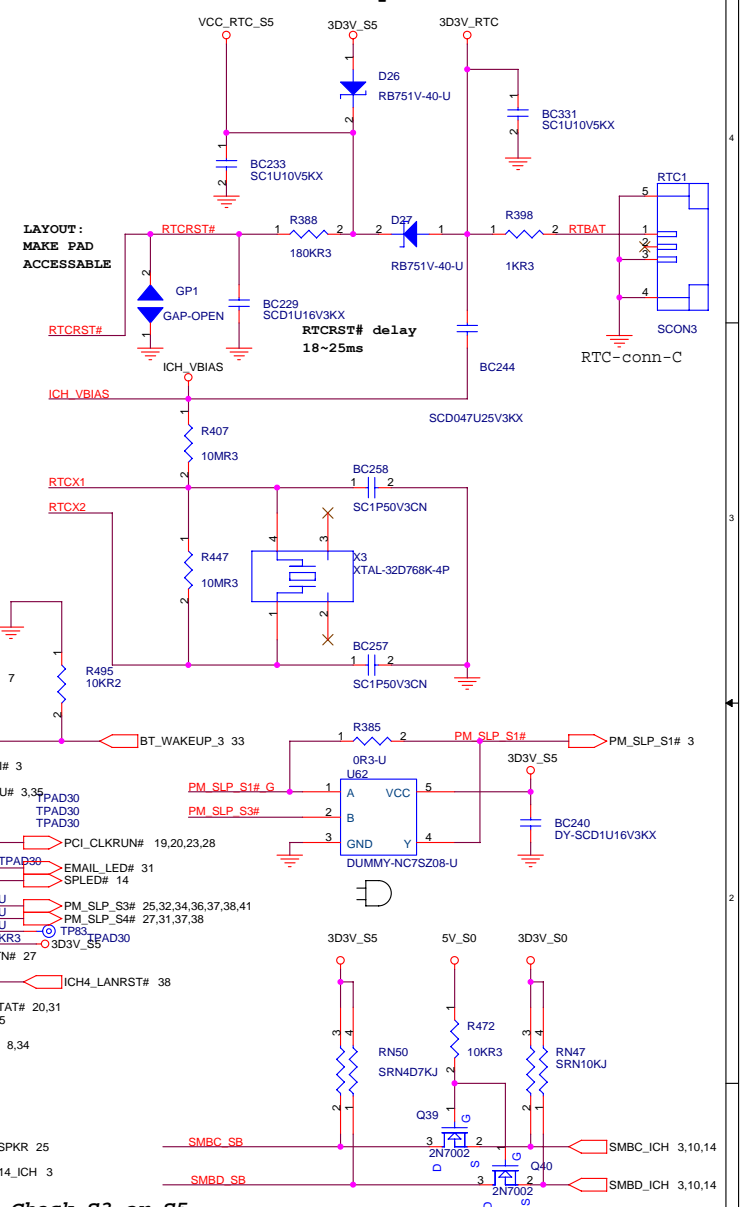


CLK termination close to ICH4

Check S3 or S5



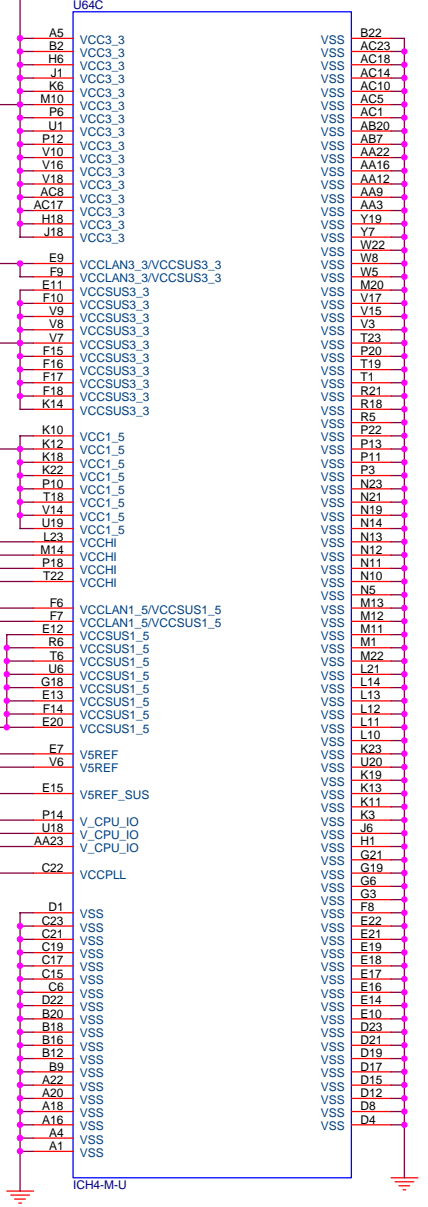
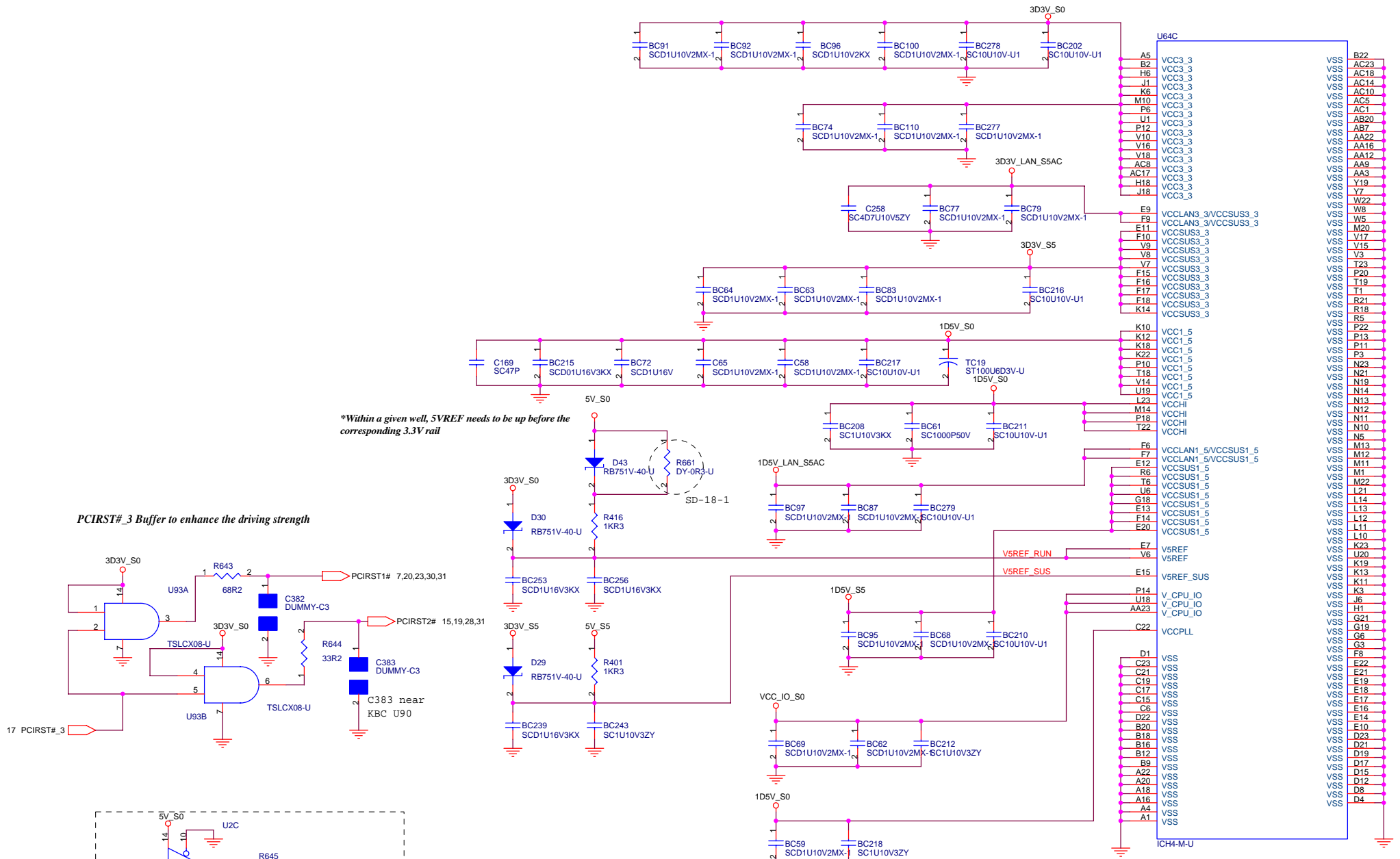
RTC Circuitry



LAYOUT: MAKE PAD ACCESSABLE

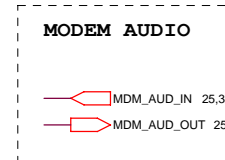
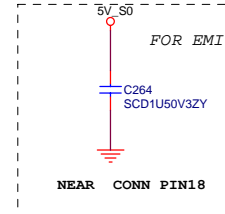
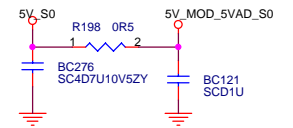
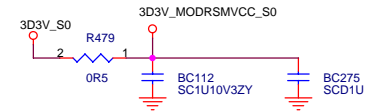
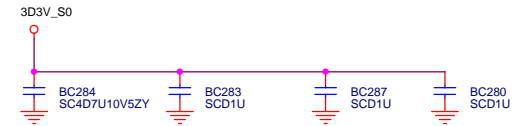
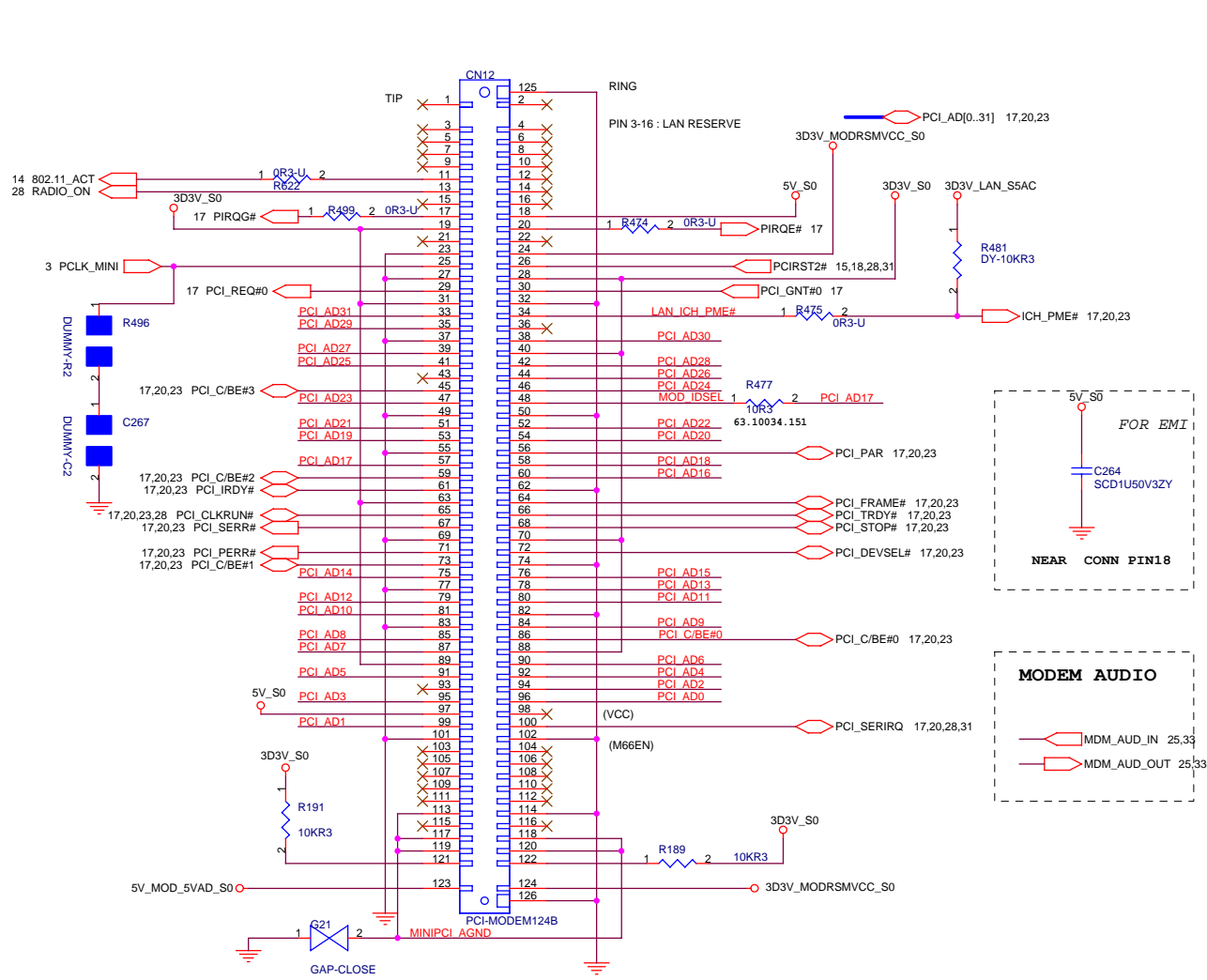
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

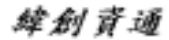
File		
ICH4-M (2 of 3)		
Size	Document Number	Rev
Custom	J2	SD
Date: Thursday, July 17, 2003	Sheet 17	of 42

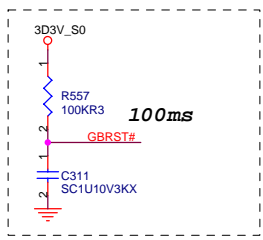


Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
ICH4-M (3 of 3)	
Size	Document Number
A3	J2
Date:	Rev
Thursday, July 17, 2003	SD
Sheet	of
18	42

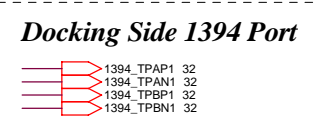
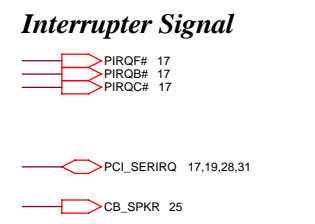
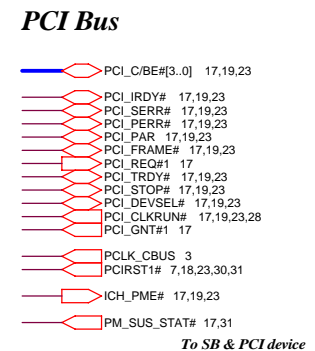
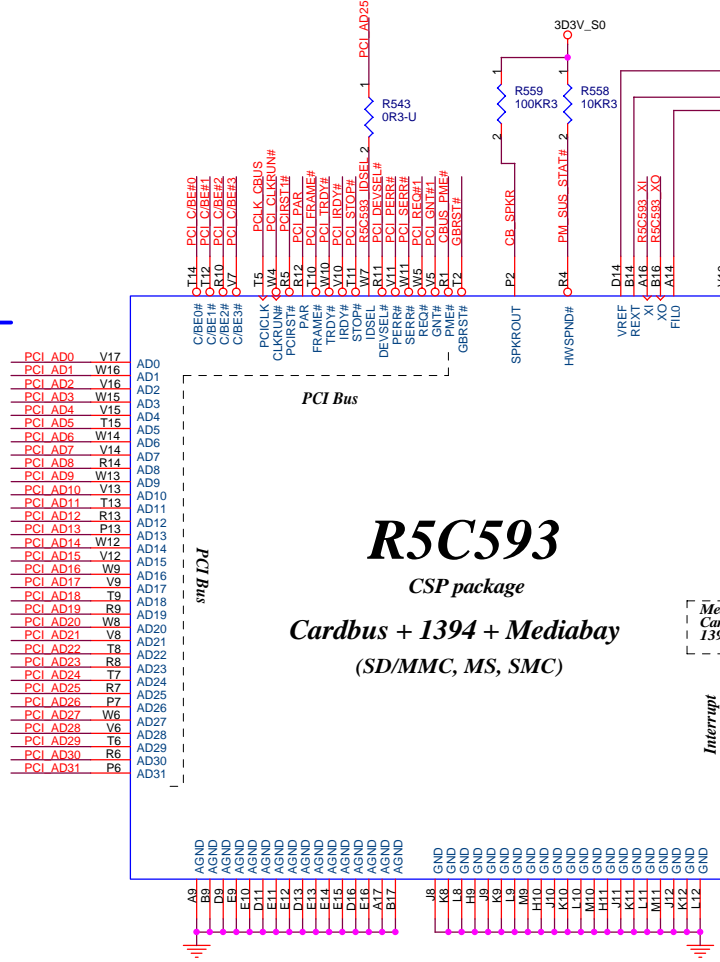
Mini PCI 802.11A/B



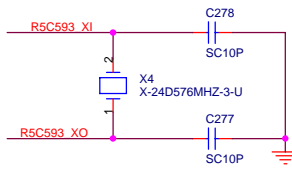
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Mini PCI Socket		
Size	Document Number	Rev
A3	J2	SD
Date:	Thursday, July 17, 2003	Sheet 19 of 42



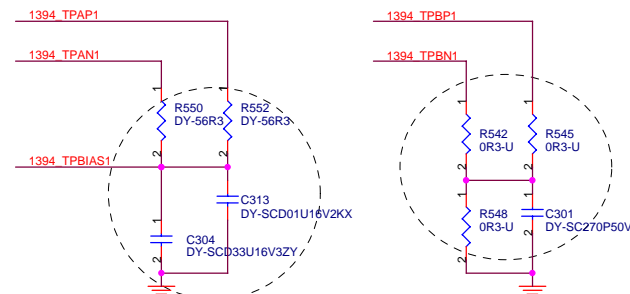
17,19,23 PCI_AD[31..0]



24.576MHz X'tal

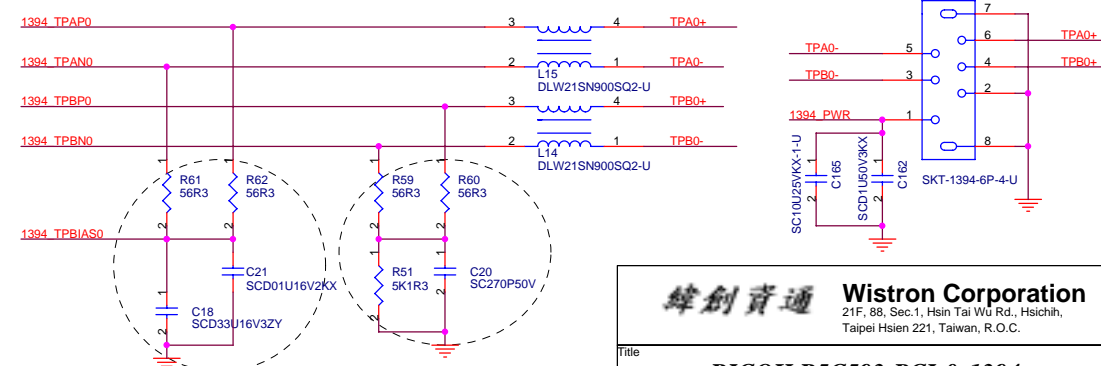


Docking Side 1394 Port



Place ACAP to Device Terminals

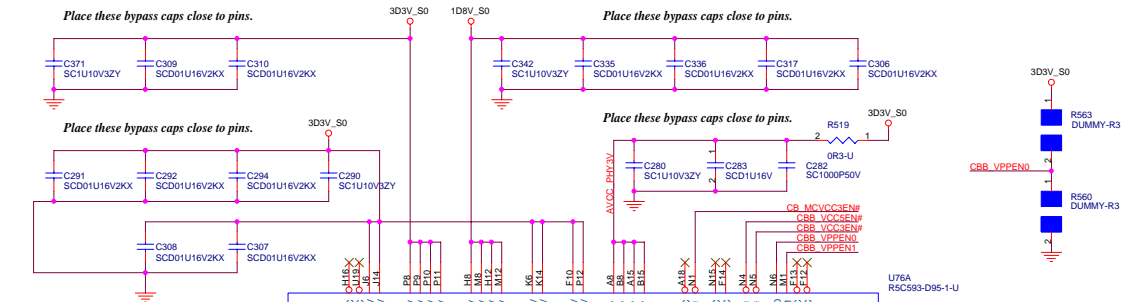
1394 Connector



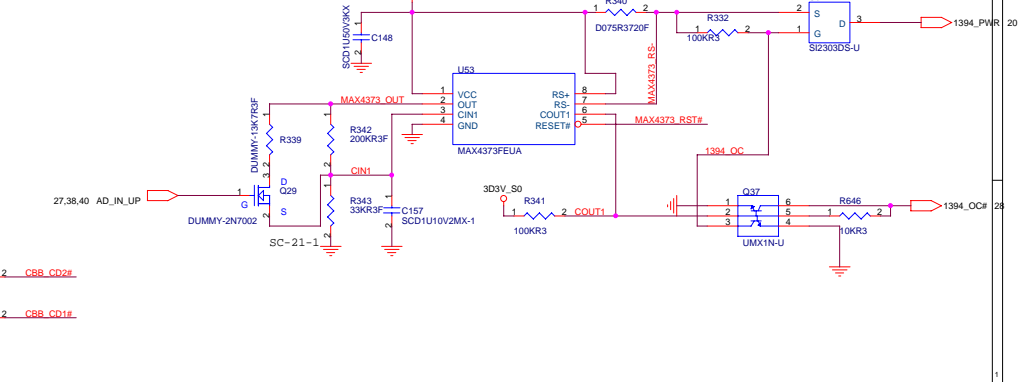
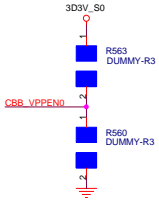
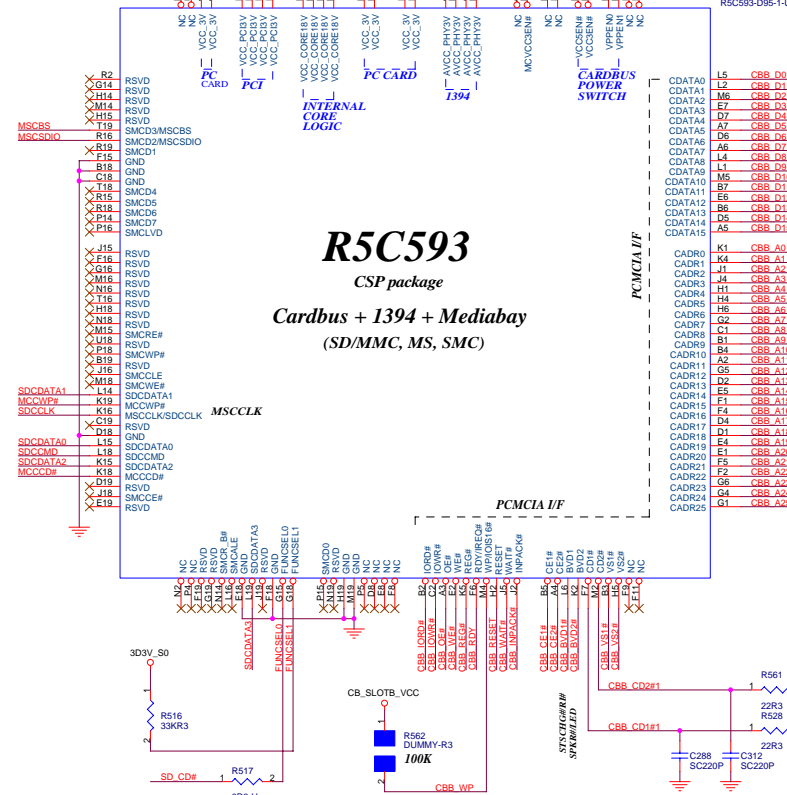
Place ACAP to Device Terminals

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
RICOH R5C593-PCI & 1394		
Size	Document Number	Rev
A3	J2	SD
Date:	Thursday, July 17, 2003	Sheet 20 of 42



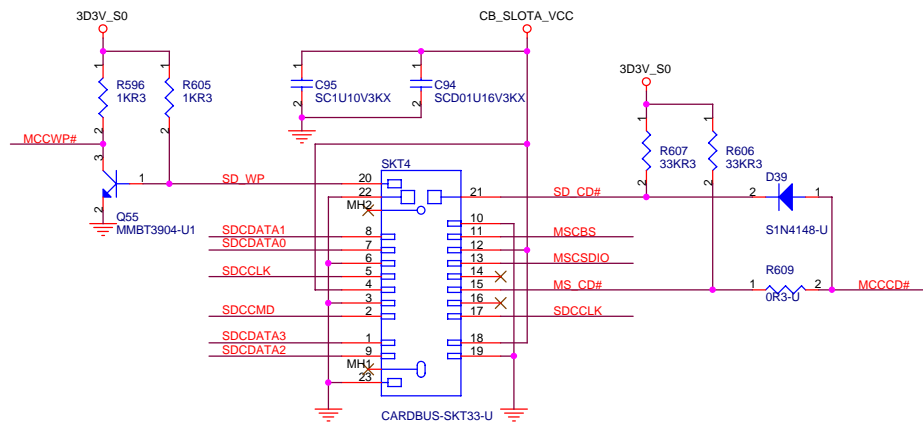
- Smart Media Card**
 - SMCD[0..7]
 - SMCCLE
 - SMCWE#
 - SMCRE#
 - SMCWP#
 - SMCC#
 - SMCR_B#
 - SMCLVD
- MMC/SD**
 - SDCDATA[0..3]
 - SDCCMD
 - SDCLK
- Memory Stick**
 - MSCCLK
 - MSCSDIO
 - MSCBS
- Common Signals**
 - MCCCD#
 - MCCWP#
- Function Select**
 - FUNSEL[1..0]



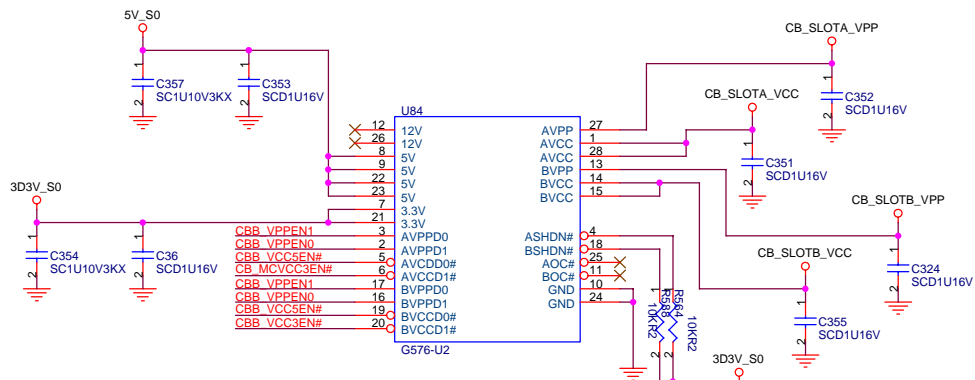
Card Insertion Detection

- Cardbus I/F**
 - CBB_D[0..15] 22
 - CBB_A[0..25] 22
 - CBB_IORD# 22
 - CBB_IOWR# 22
 - CBB_OE# 22
 - CBB_WE# 22
 - CBB_REG# 22
 - CBB_RDY 22
 - CBB_WP 22
 - CBB_RESET 22
 - CBB_WAIT# 22
 - CBB_INPACK# 22
 - CBB_CE1# 22
 - CBB_CE2# 22
 - CBB_BVD1# 22
 - CBB_BVD2# 22
 - CBB_CD1# 22
 - CBB_CD2# 22
 - CBB_VS1# 22
 - CBB_VS2# 22
- Power Switch I/F**
 - CBB_VCCSEN# 22
 - SD_CEN 22
 - CBB_VPPEN0 22
 - CBB_VPPEN1 22
 - CB_MCVCCEN# 22
- MMC/SD**
 - SDCDATA[0..3] 22
 - SD_CEN 22
 - SDCCMD 22
 - SDCLK 22
- Memory Stick**
 - MSCCLK => SDCLK
 - MSCBS 22
 - MSCSDIO 22
- Common Signals**
 - MCCCD# 22
 - MCCWP# 22
 - MAX4373_RST# 28

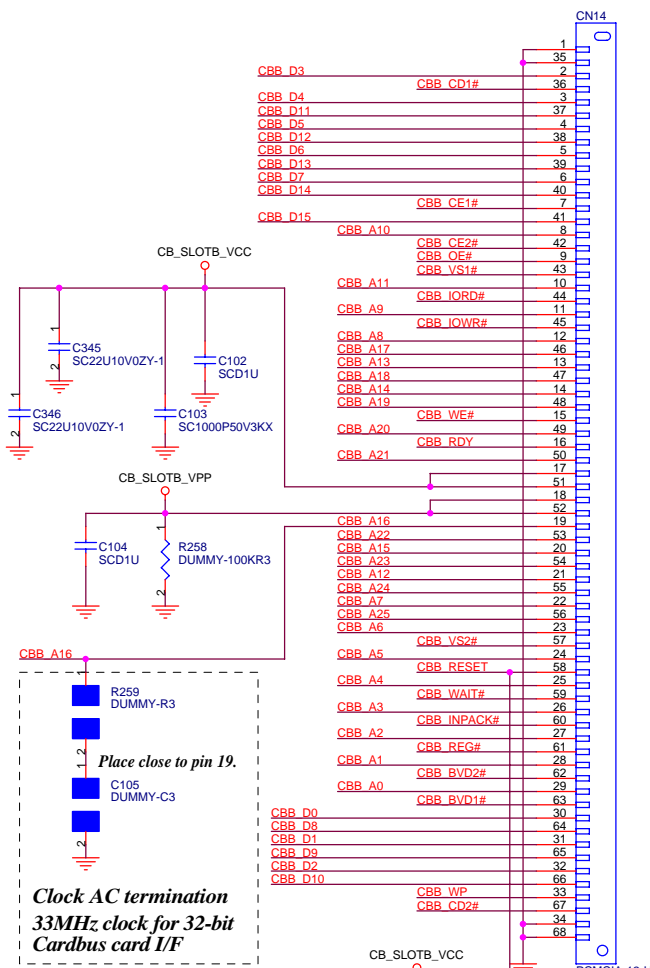
MediaBay Socket



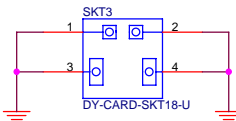
Cardbus Power Switch



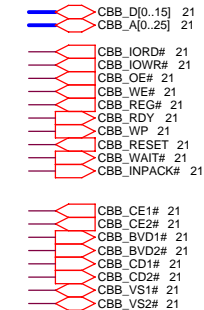
PCMCIA Socket



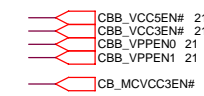
Cardbus Cage



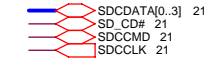
Cardbus I/F



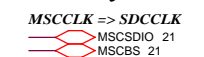
Power Switch I/F



MMC/SD



Memory Stick



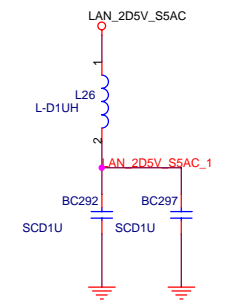
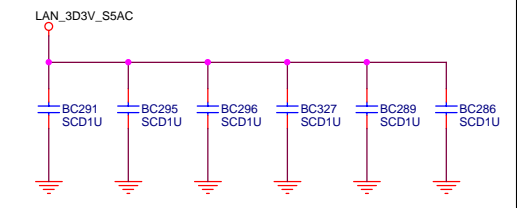
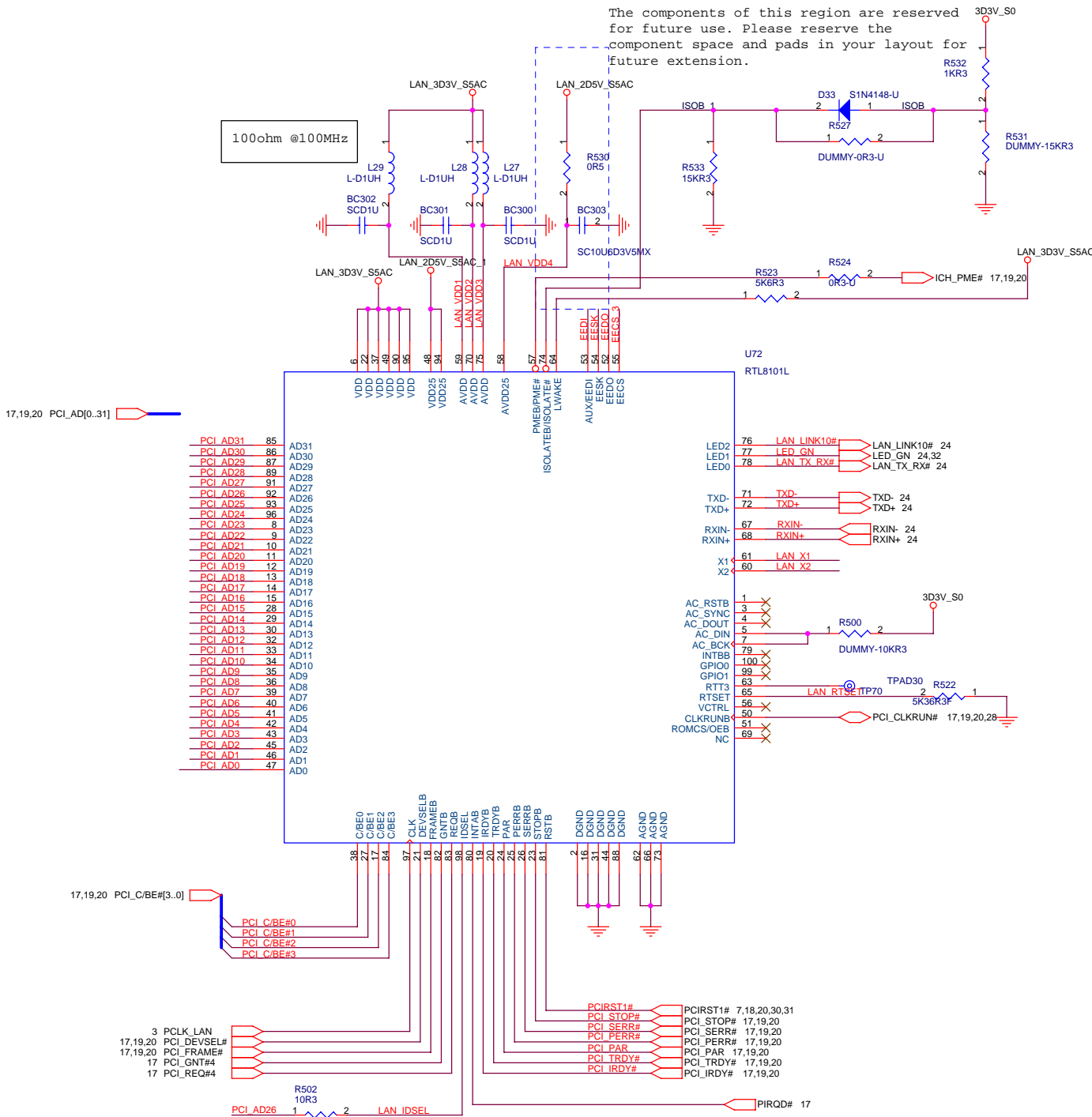
Common Signals



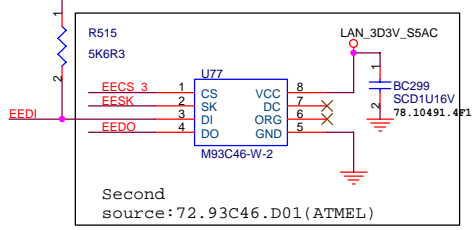
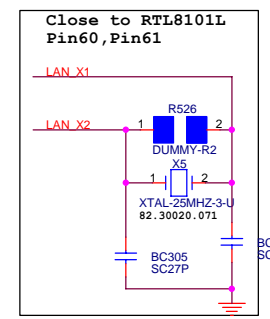
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
R5C593-Pcmcia & Mediabay Sockets		
Size	Document Number	Rev
A3		SD
Date:	Thursday, July 17, 2003	Sheet 22 of 42

The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.



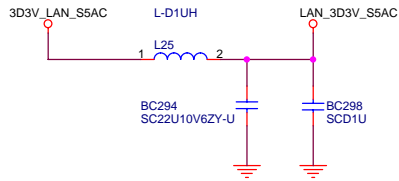
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



Second source: 72.93C46.D01 (ATMEL)
main source: 72.93C46.E01

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN		
Size: A3	Document Number: J2	Rev: SD
Date: Thursday, July 17, 2003	Sheet: 23 of 42	

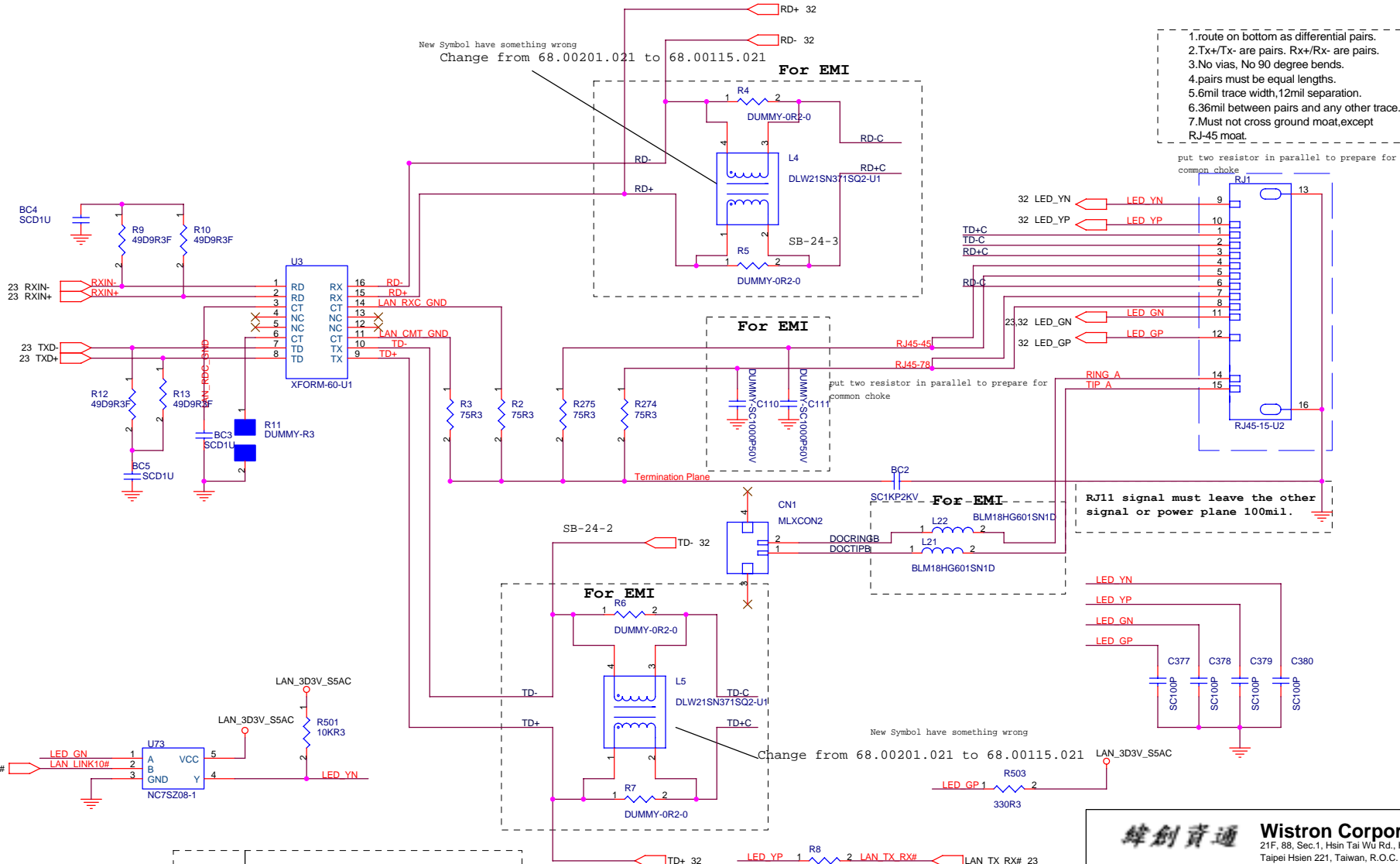
*For RTL8101 application, all bead must be rated 300mA/100ohm@100MHz



New Symbol have something wrong
Change from 68.00201.021 to 68.00115.021

For EMI

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



put two resistor in parallel to prepare for common choke

RJ11 signal must leave the other signal or power plane 100mil.

LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX
LED1	LINK100	LINK10/100	LINK10/100	LINK100
LED2	LINK10	FULL	RX	LINK10

Green LED: Speed 100: ON/Speed 10: OFF
Yellow LED: Link : ON, TX/RX:
Flash (10Hz)

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Title: **LAN Connector**

Size A3	Document Number	J2	Rev SD
Date: Thursday, July 17, 2003		Sheet 24	of 42

CS4299-XQ AC97 AUDIO CODEC

AC'97

- AC_SDATA_DOUT 16
- AC_BITCLK 16,33
- AC_SDATA_IN0 16
- AC_SYNC 16
- CODEC_AC_RST# 16
- To SB

Audio signal

- MDM_AUD_IN 33
- MDM_AUD_OUT 33

To MDC & MiniPCI

- SB_SPKR 17

To SB

- SOUNDL 26
- SOUNDR 26
- LINE_IN_R 26
- LINE_IN_L 26

To OP-Amp

- MIC_IN 26

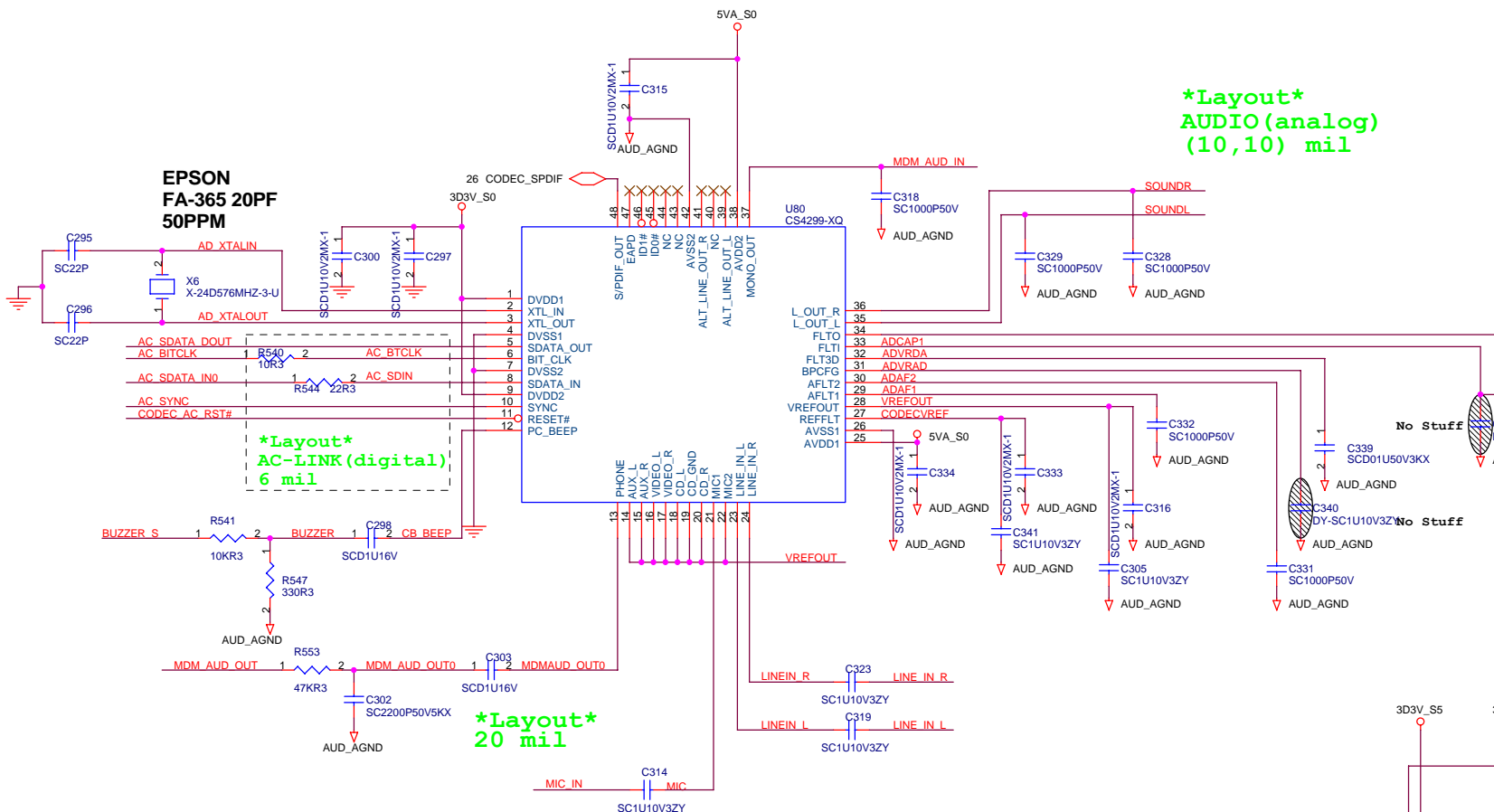
To Microphone

- CB_SPKR 20

To CardBus

- KBC_SPKR 31

To KBC



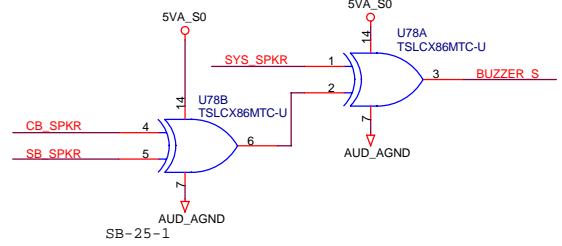
***Layout*
AC-LINK (digital),
6 mil**

***Layout*
20 mil**

***Layout*
AUDIO (analog)
(10,10) mil**

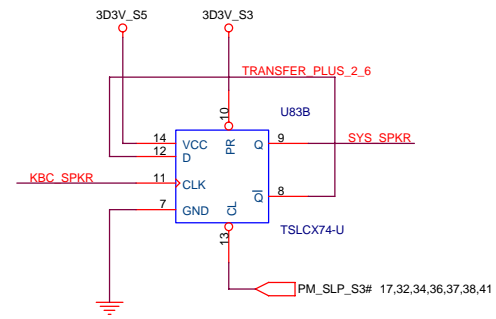
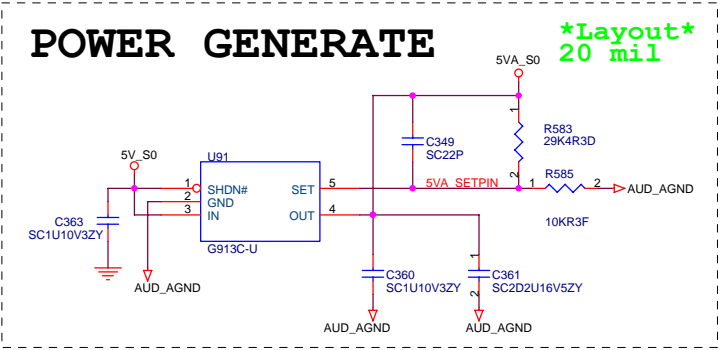
BEEP SOUND LOGIC

Layout
locate near audio
moat opening 6
mil

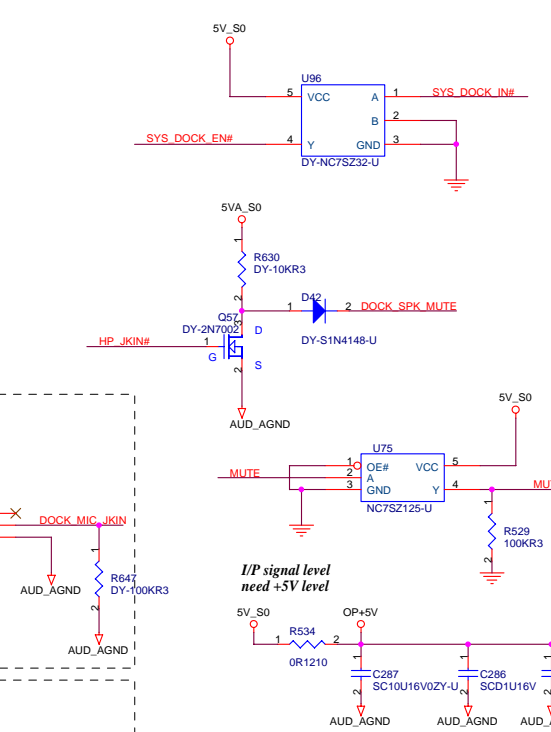
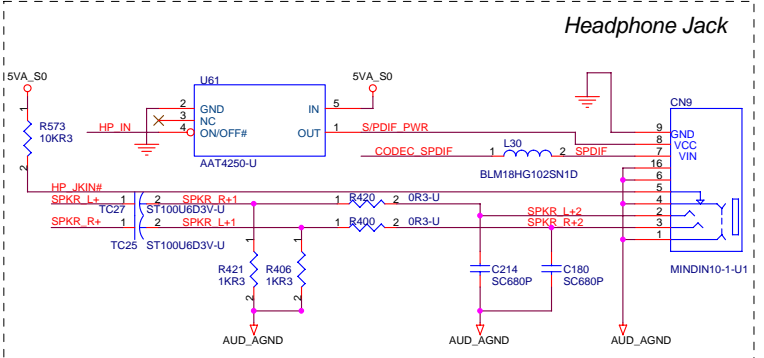
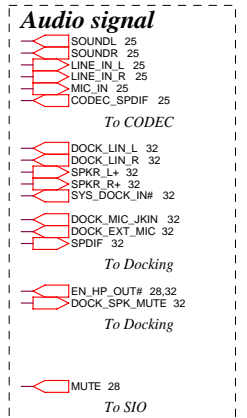
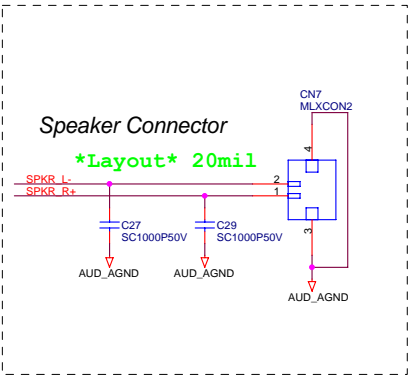
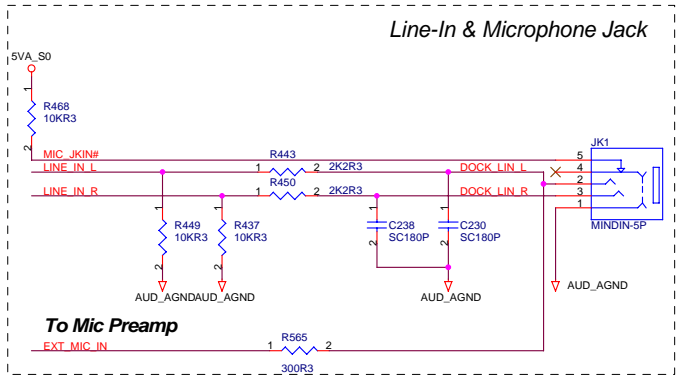
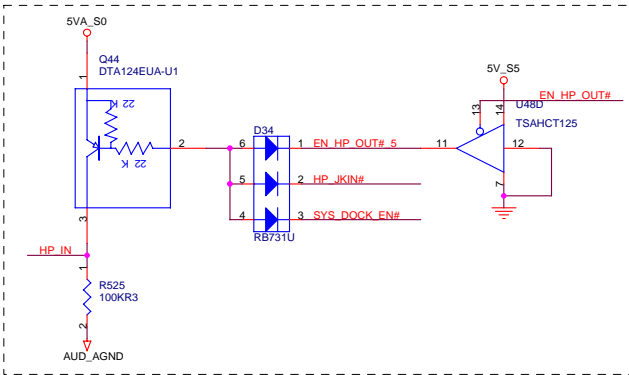


POWER GENERATE

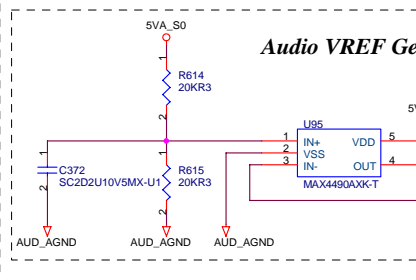
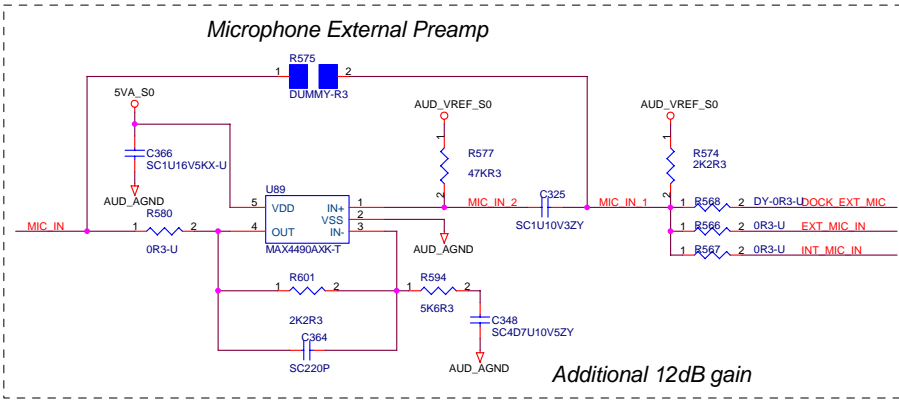
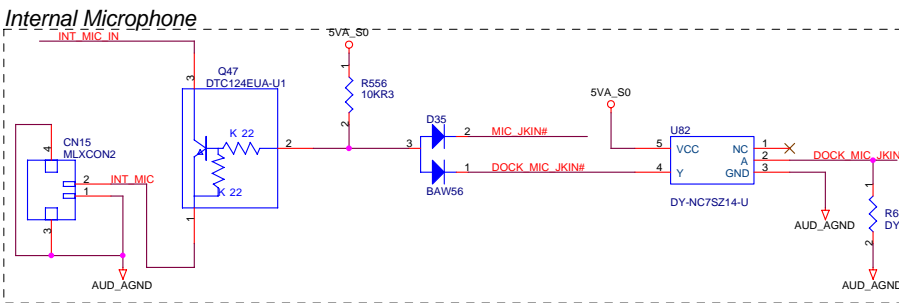
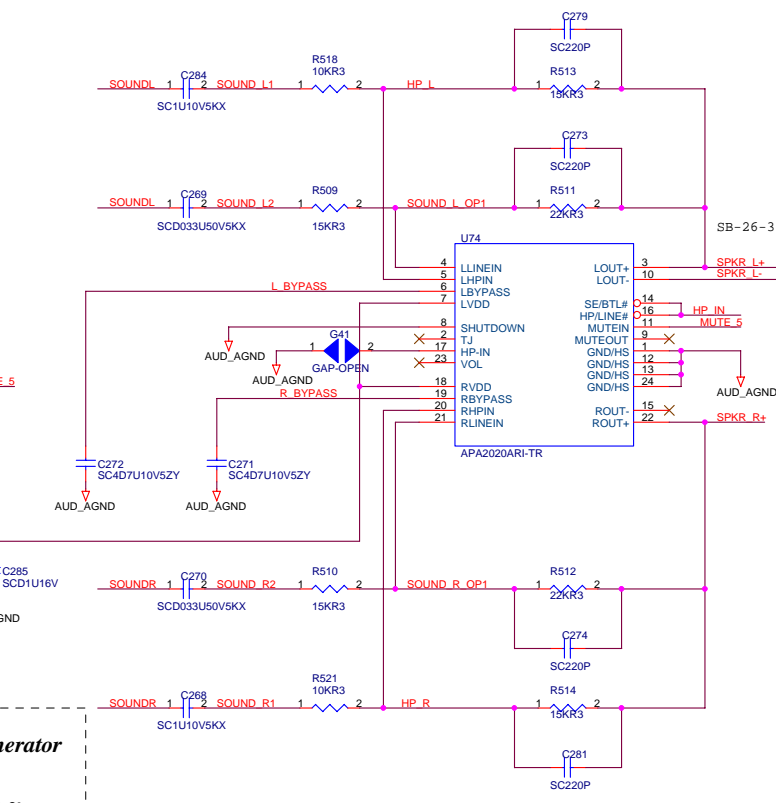
***Layout*
20 mil**



緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title AC'97 CODEC - CS4299	
Size A3	Document Number J2
Date: Tuesday, August 26, 2003	Sheet 25 of 42
	Rev SD



AUDIO OP AMPLIFIER



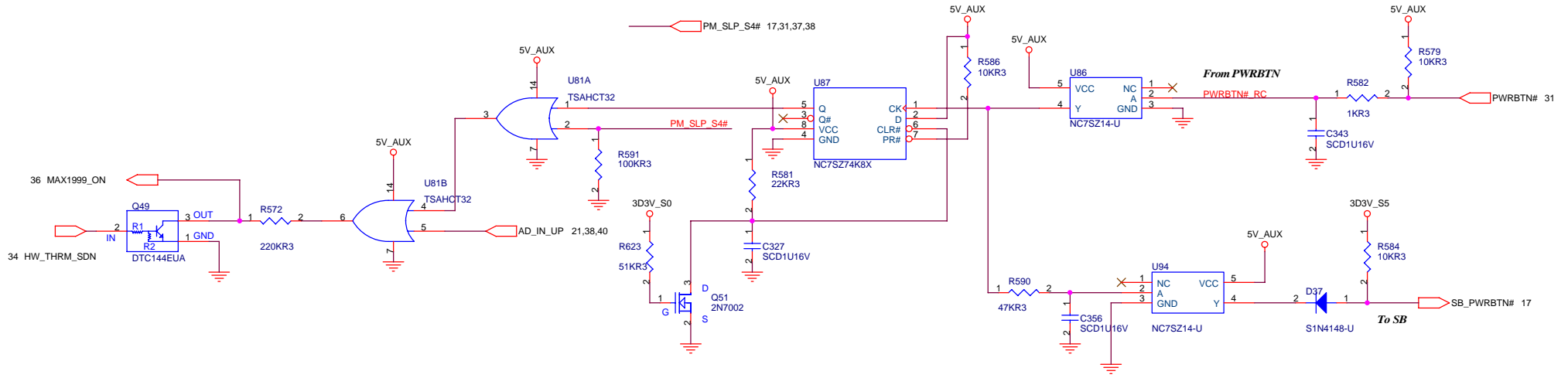
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio AMP and Jack**

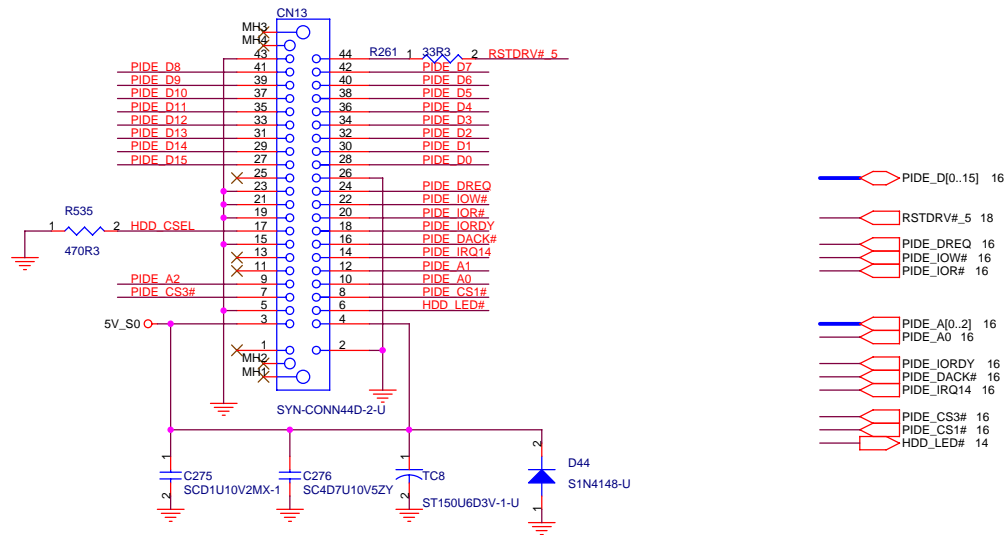
Size: Custom
 Document Number: **J2**
 Date: Thursday, July 17, 2003

Rev: **SD**
 Sheet 26 of 42

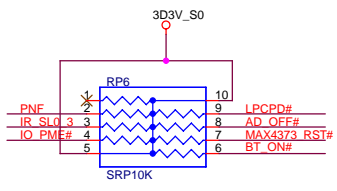
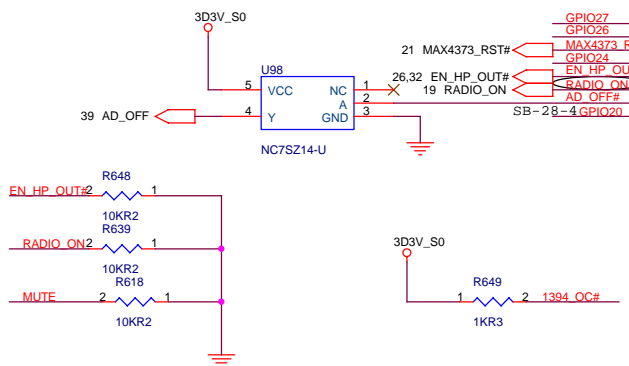
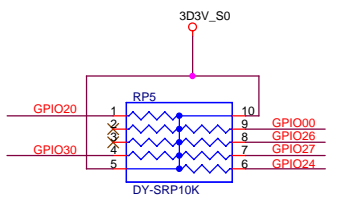
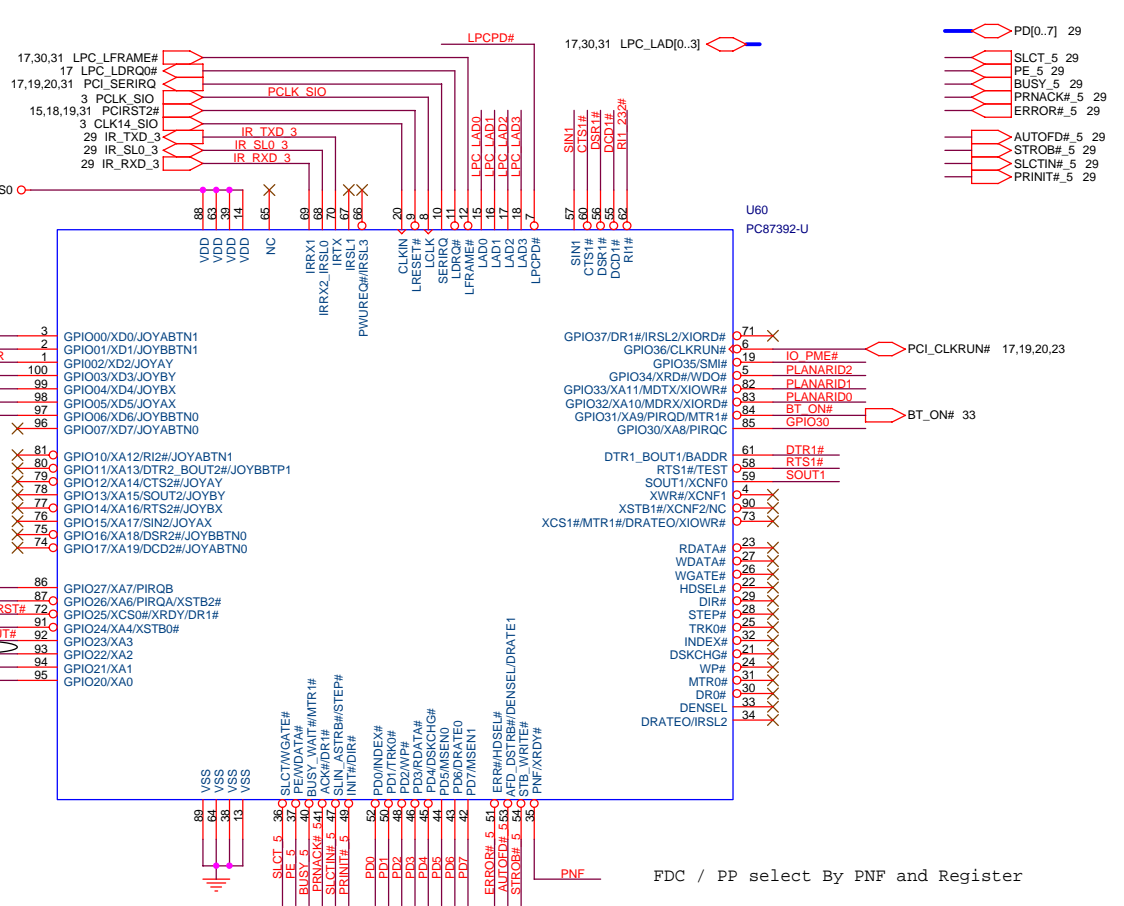
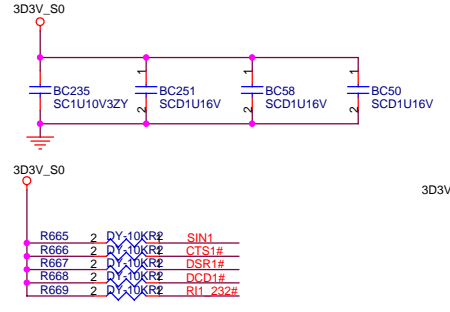
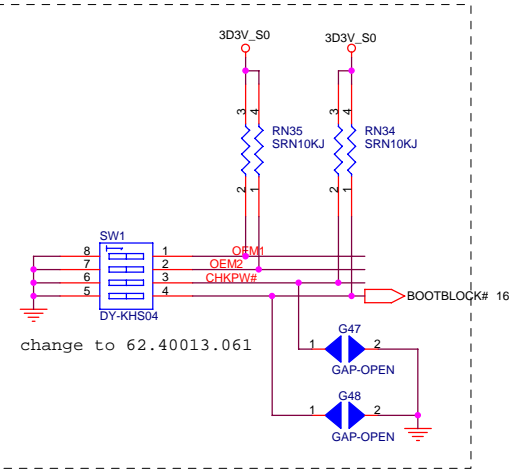
Power ON Circuit



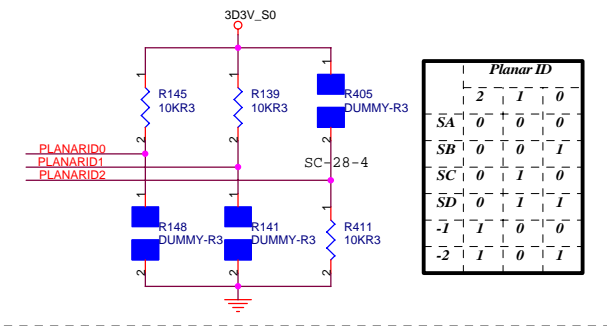
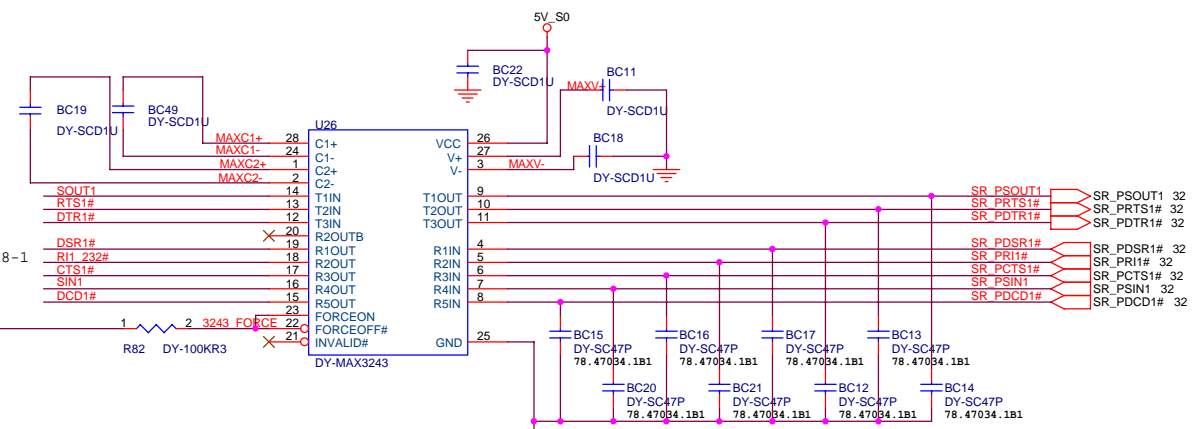
HDD CONN



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Title	
HDD/Power ON Circuit	
Size	Document Number
A3	J2
Date:	Rev
Thursday, July 17, 2003	SD
Sheet	of
27	42



SERIAL PORT



Planar ID			
2	1	0	
SA	0	0	0
SB	0	0	1
SC	0	1	0
SD	0	1	1
-1	1	0	0
-2	1	0	1

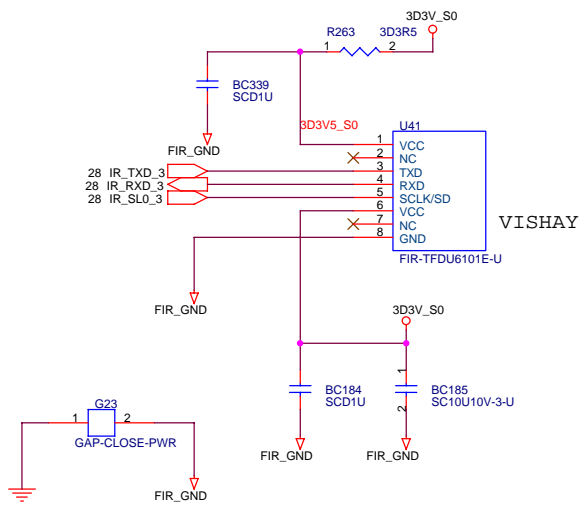
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SIO**

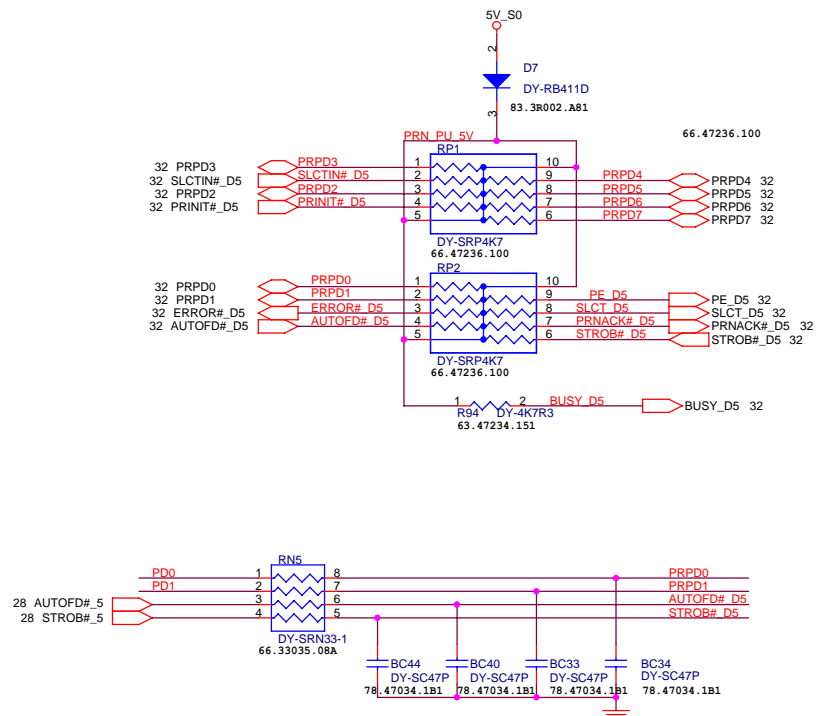
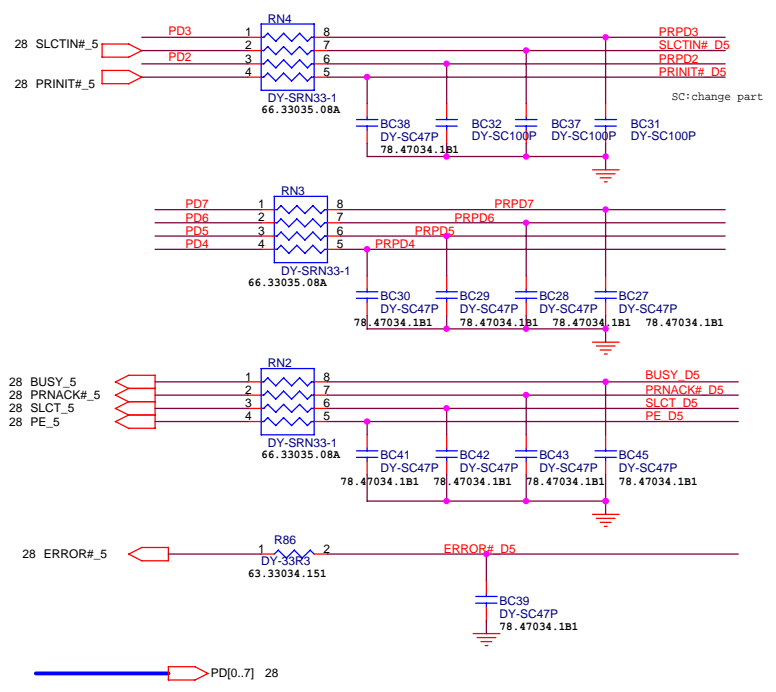
Size: A3 Document Number: **J2** Rev: **SD**

Date: Thursday, July 17, 2003 Sheet 28 of 42

FIR



PRINTER PORT



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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title Printer/FIR

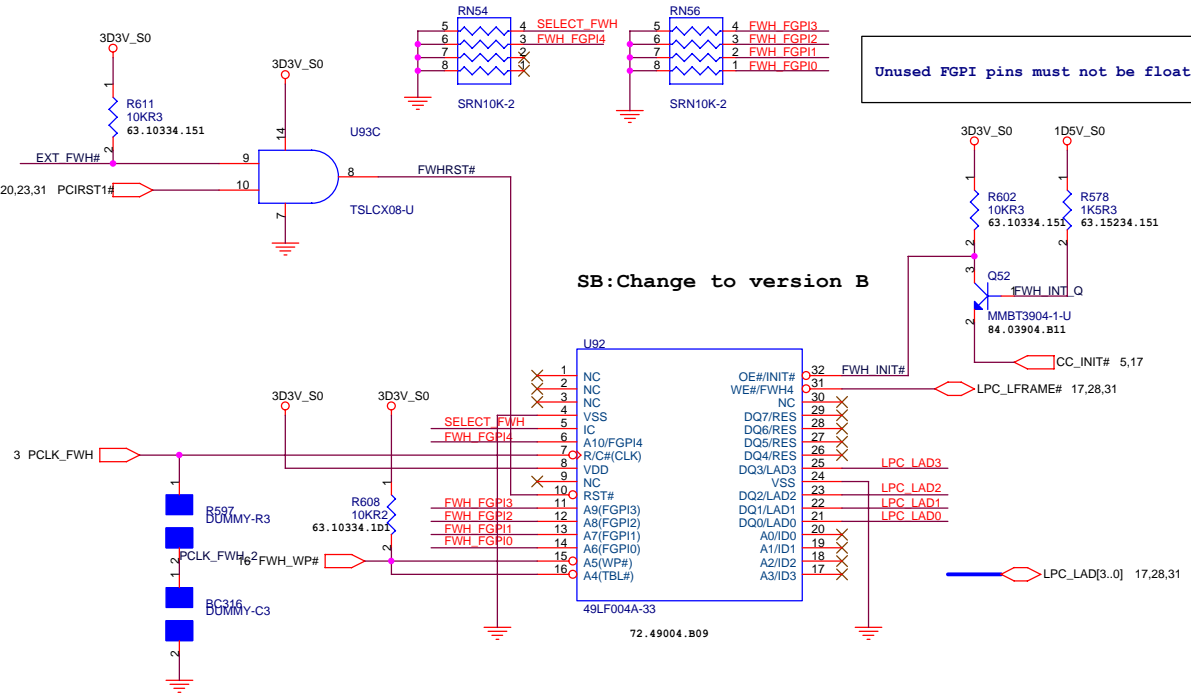
Size A3 Document Number J2 Rev SD

Date: Thursday, July 17, 2003 Sheet 29 of 42

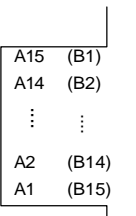
Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46

Unused FGPI pins must not be float

SB: Change to version B

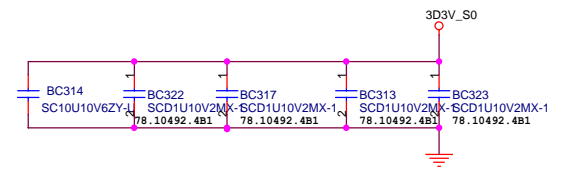
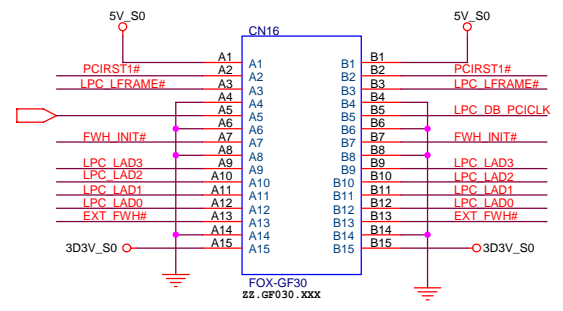


TOP VIEW



(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

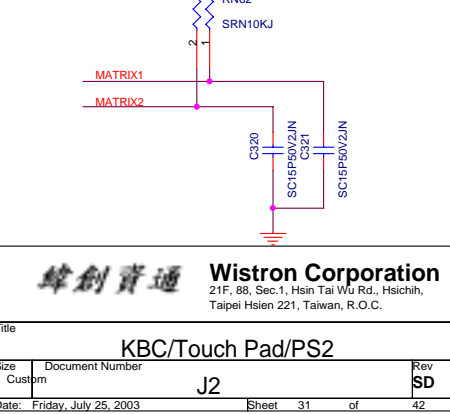
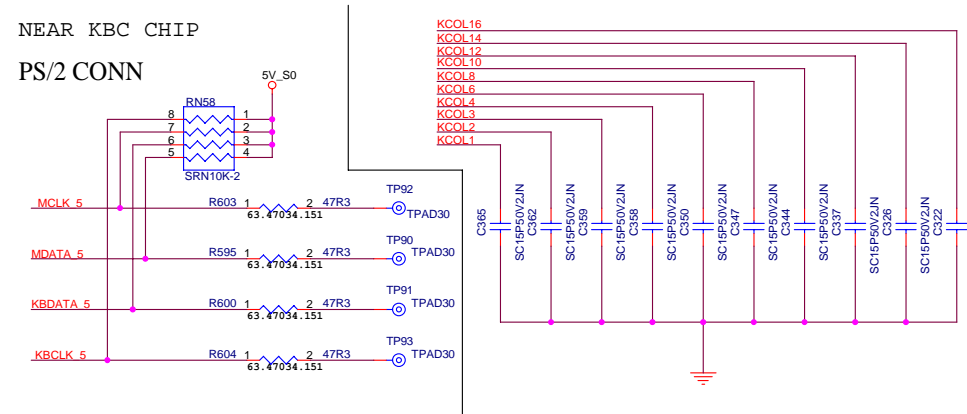
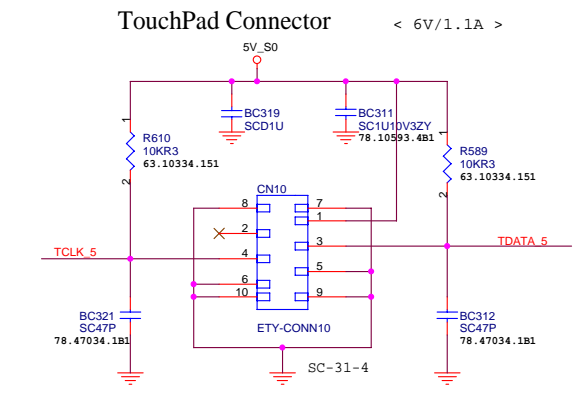
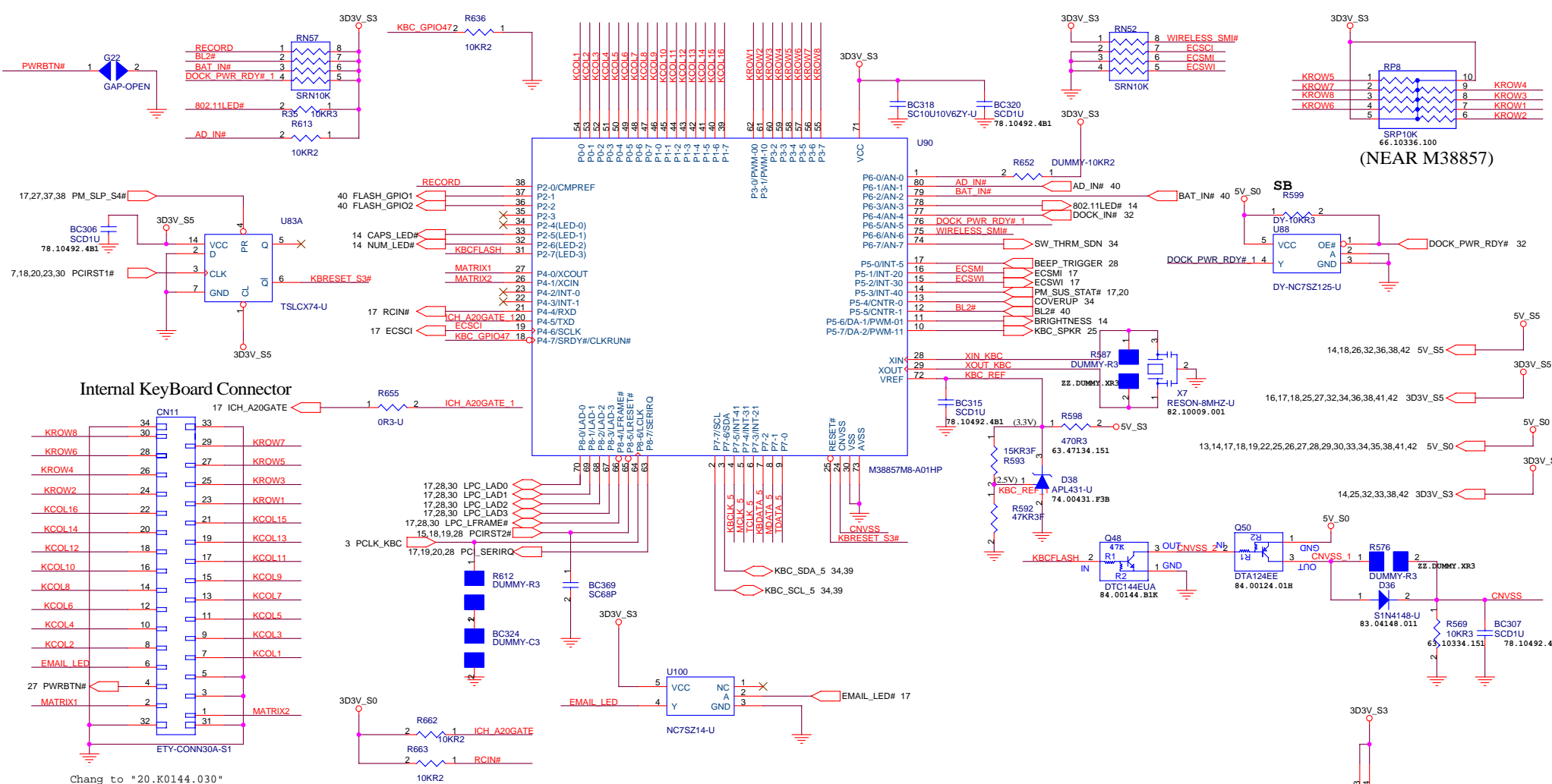


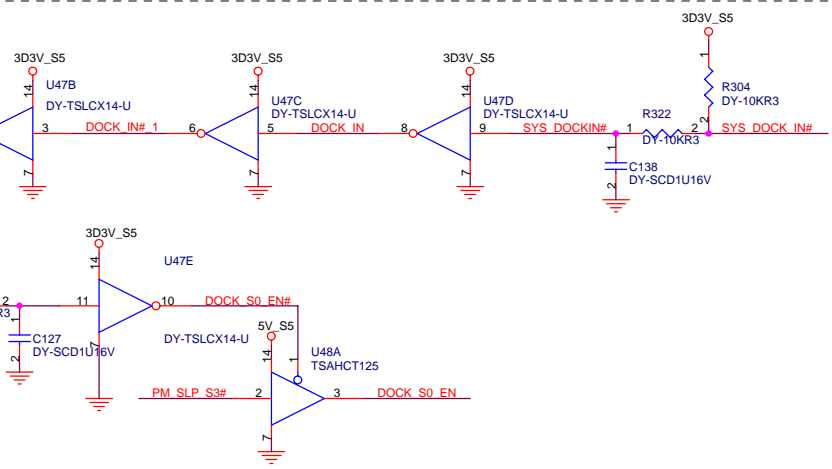
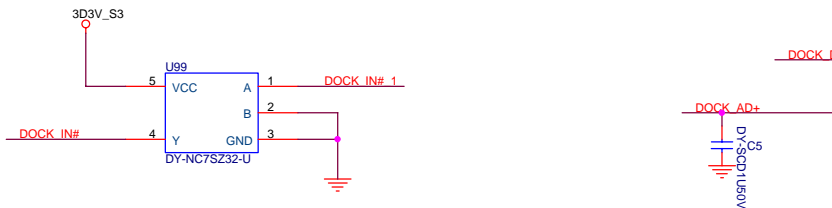
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH/Debug Port

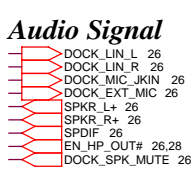
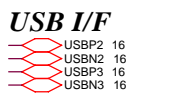
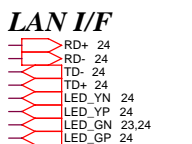
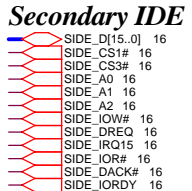
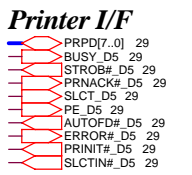
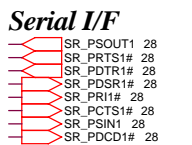
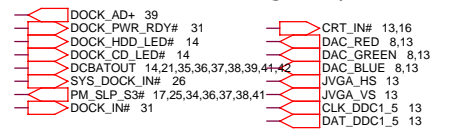
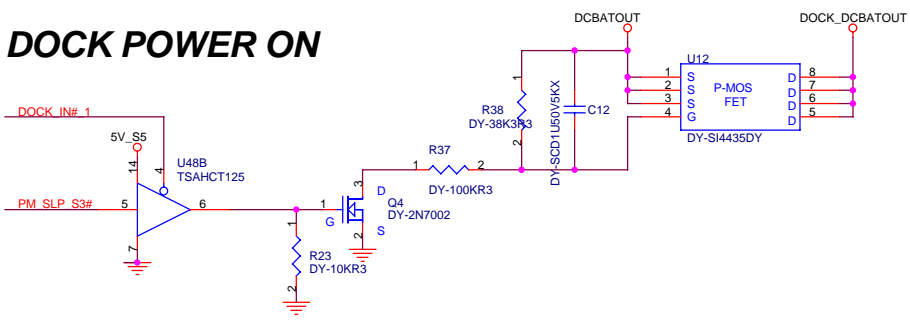
Size: A3 Document Number: J2 Rev: SD

Date: Thursday, July 17, 2003 Sheet: 30 of 42





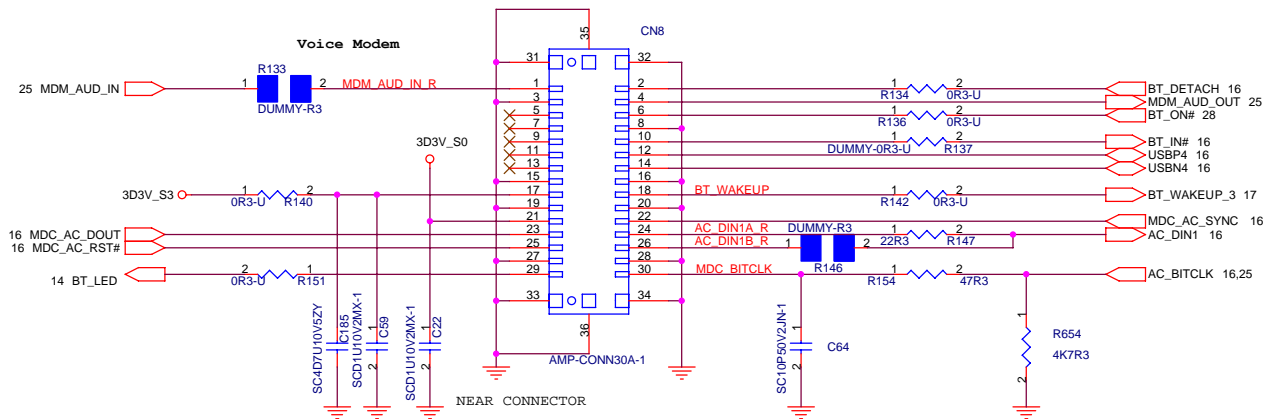
DOCK POWER ON



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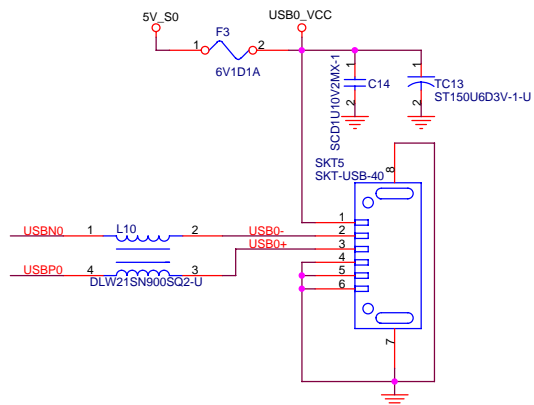
Title DOCKING		
Size A3	Document Number J2	Rev SD
Date: Thursday, July 17, 2003	Sheet 32	of 42

MDC CONN

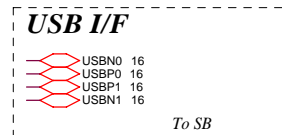
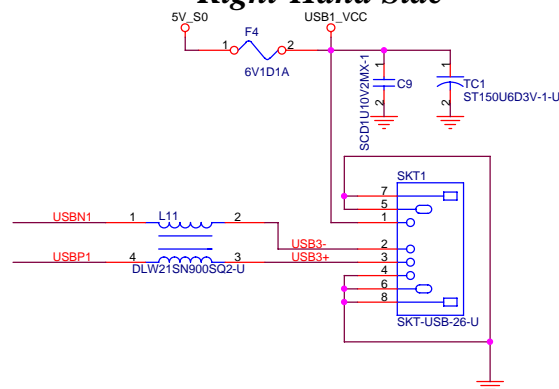


USB PORT

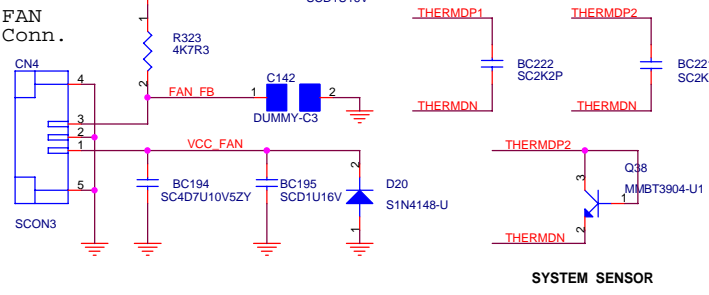
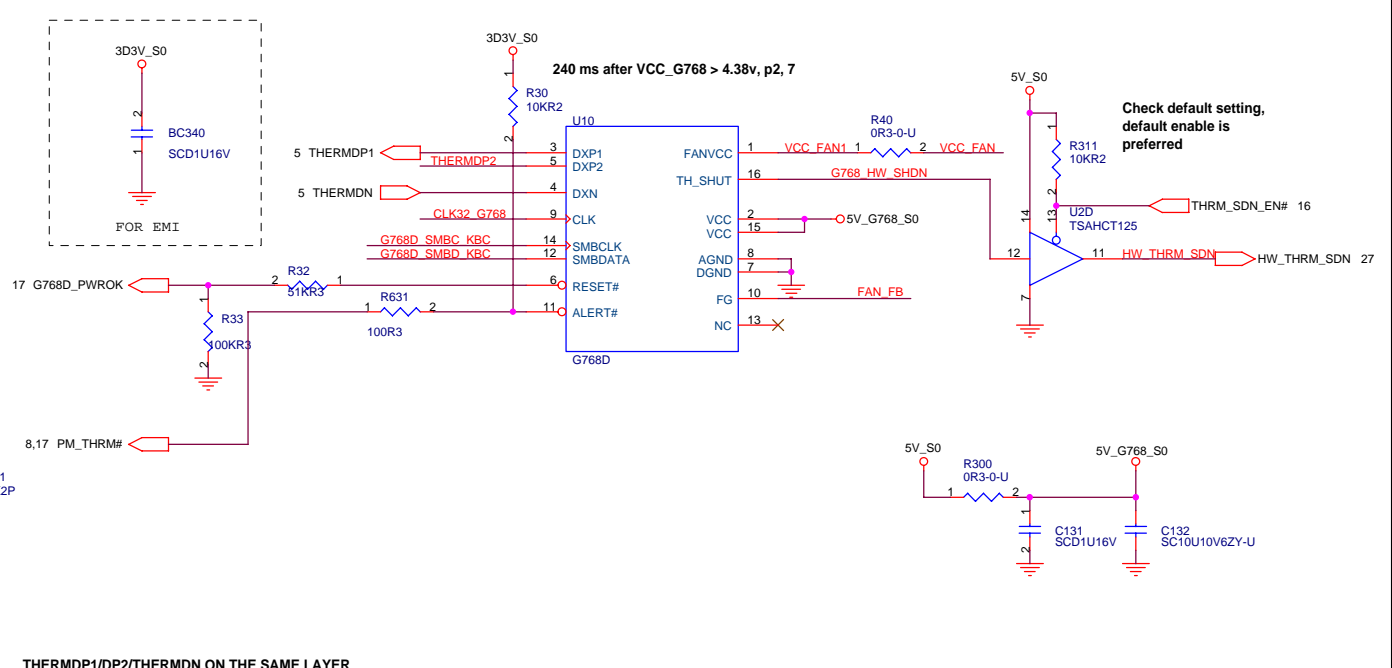
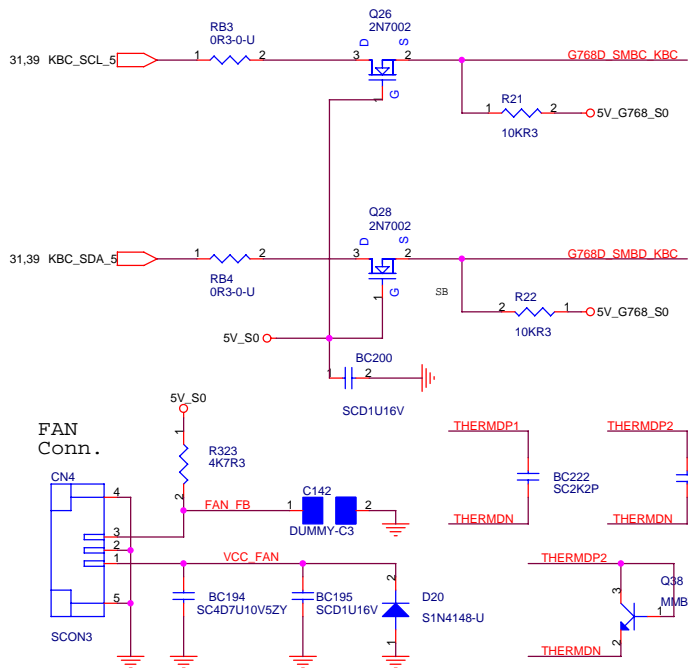
Left-Hand Side



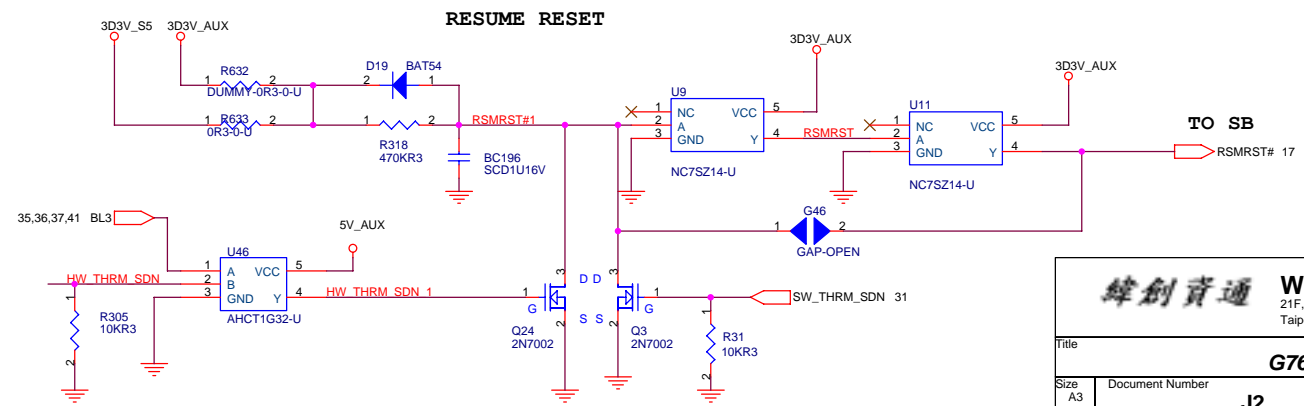
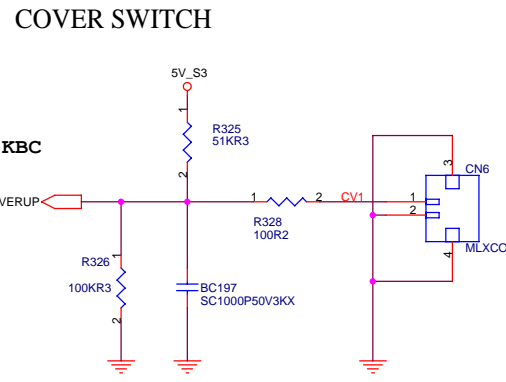
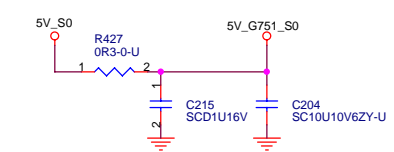
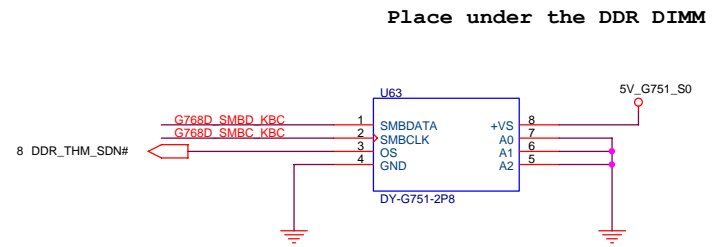
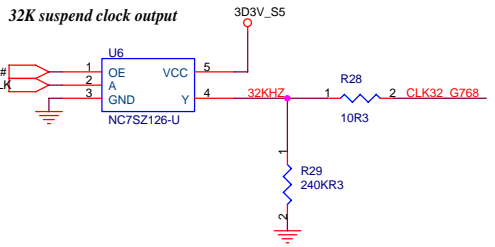
Right-Hand Side



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title MDC CONN & USB CONN			
Size A3	Document Number J2		Rev SD
Date: Thursday, July 17, 2003	Sheet	33	of 42



THERMDP1/DP2/THERMDN ON THE SAME LAYER
 W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
 CAPS CLOSE TO G768D



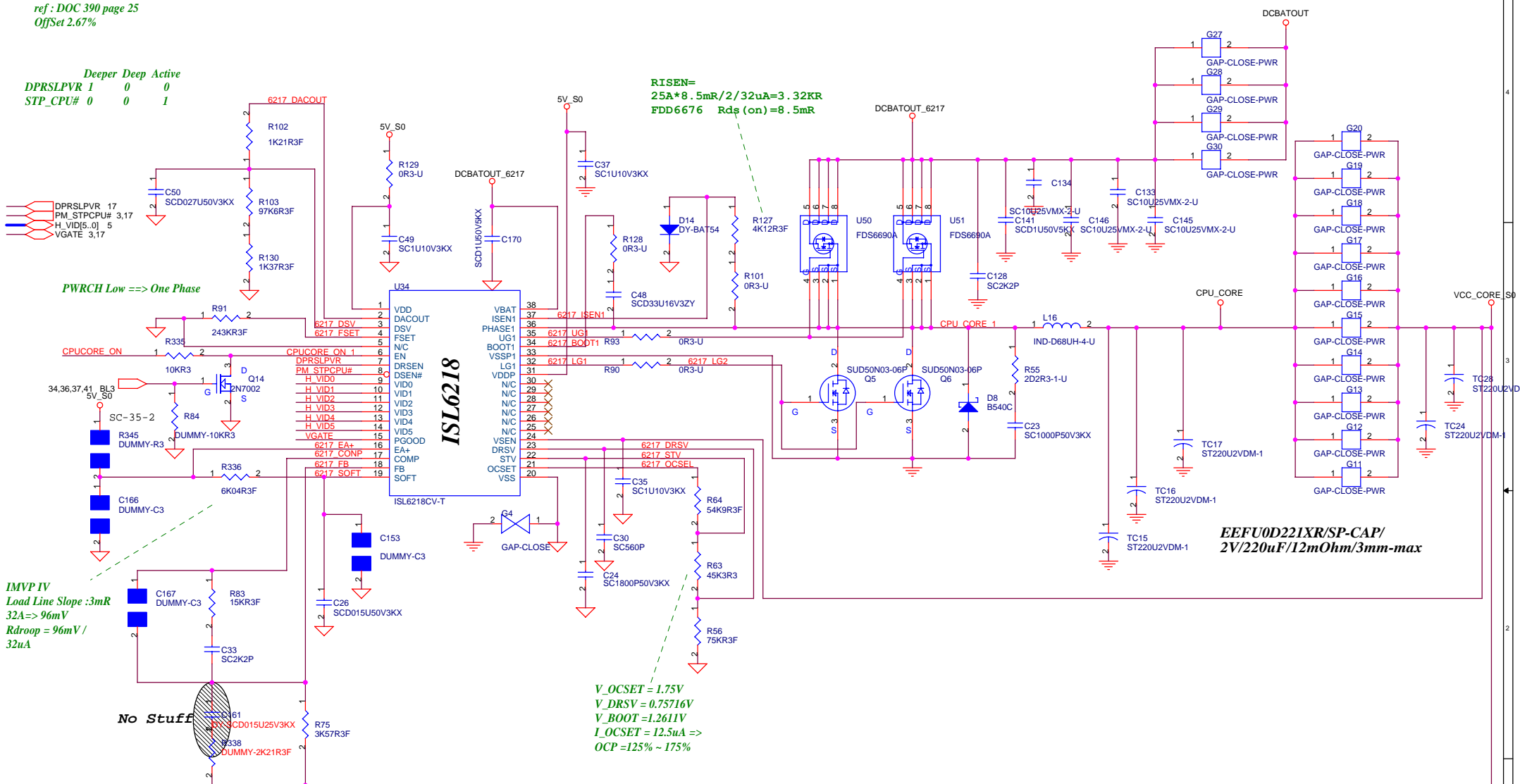
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title G768D	
Size A3	Document Number J2
Date: Thursday, July 17, 2003	Rev SD
Sheet 34	of 42

Deep_Sleep
 93.1k/(93.1k+2.55k)=97.334%
 ref : DOC 390 page 25
 OffSet 2.67%

Deeper Deep Active
 DPRSLPVR 1 0 0
 STP_CPU# 0 0 1

RISEN=
 $25A * 8.5mR / 2 / 32uA = 3.32KR$
 FDD6676 Rds(on) = 8.5mR

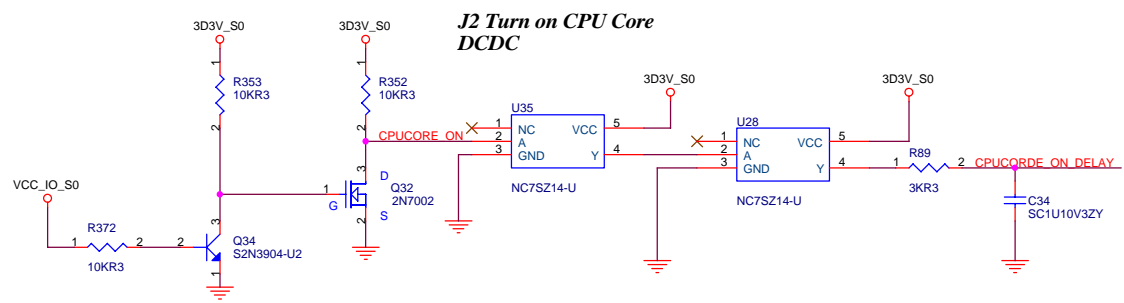
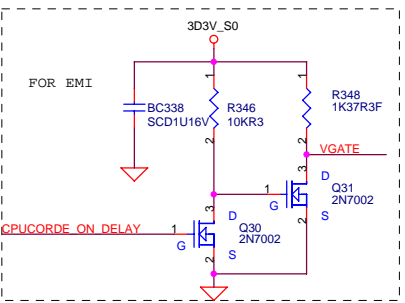
PWRCH Low ==> One Phase



IMVP IV
 Load Line Slope : 3mR
 32A => 96mV
 Rdroop = 96mV / 32uA

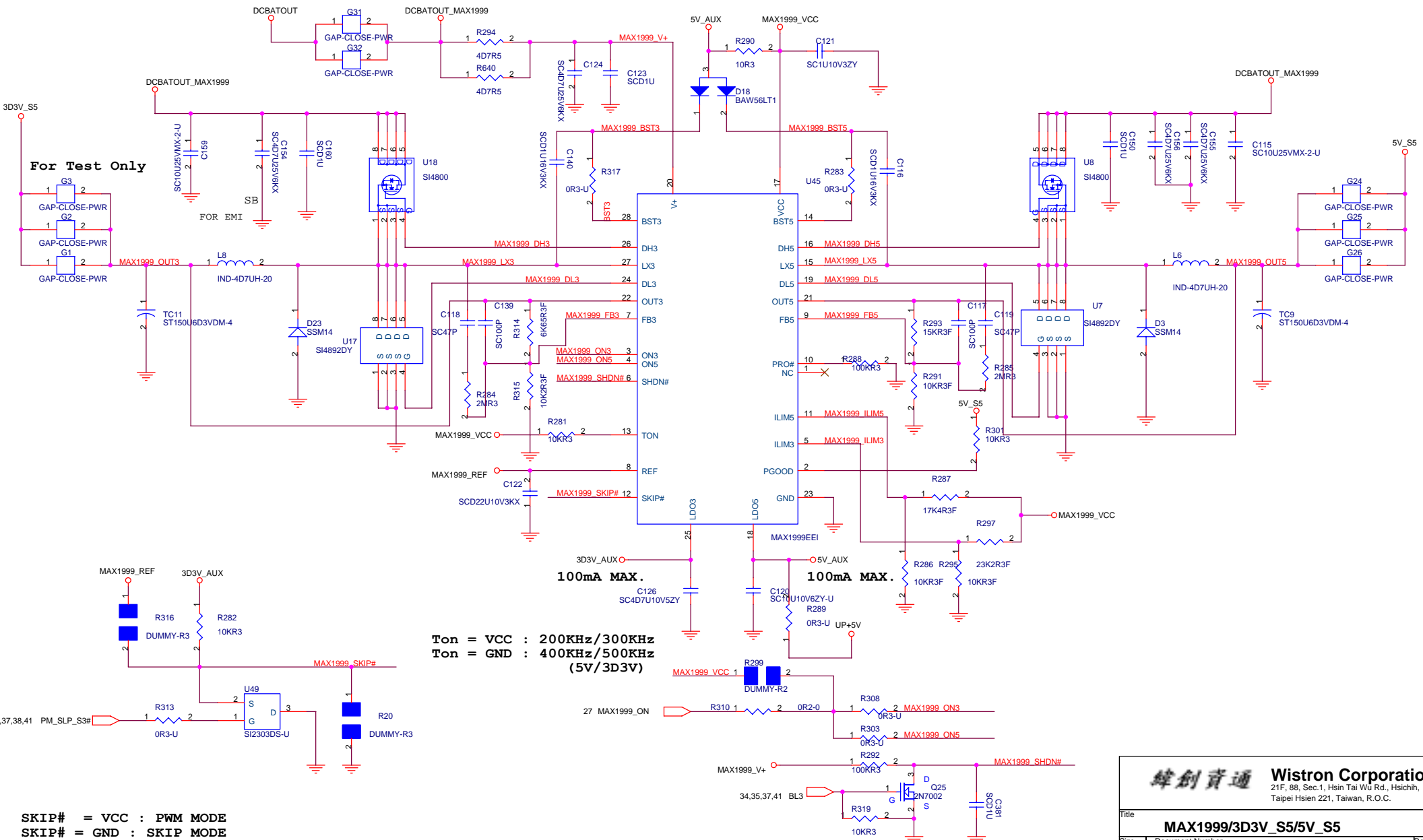
V_OCSET = 1.75V
 V_DRVS = 0.75716V
 V_BOOT = 1.2611V
 I_OCSET = 12.5uA =>
 OCP = 125% - 175%

EEFU0D221XR/SP-CAP/
 2V/220uF/12mOhm/3mm-max



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Title	
IMVP IV-CPU POWER-ISL6217	
Size	Document Number
A3	J2
Date: Thursday, July 17, 2003	Sheet 35 of 42
	Rev SD

SYSTEM DC/DC 3D3V_S5/5V_S5

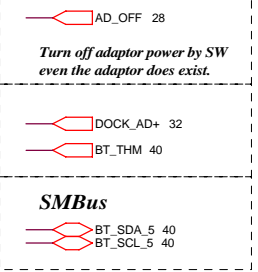
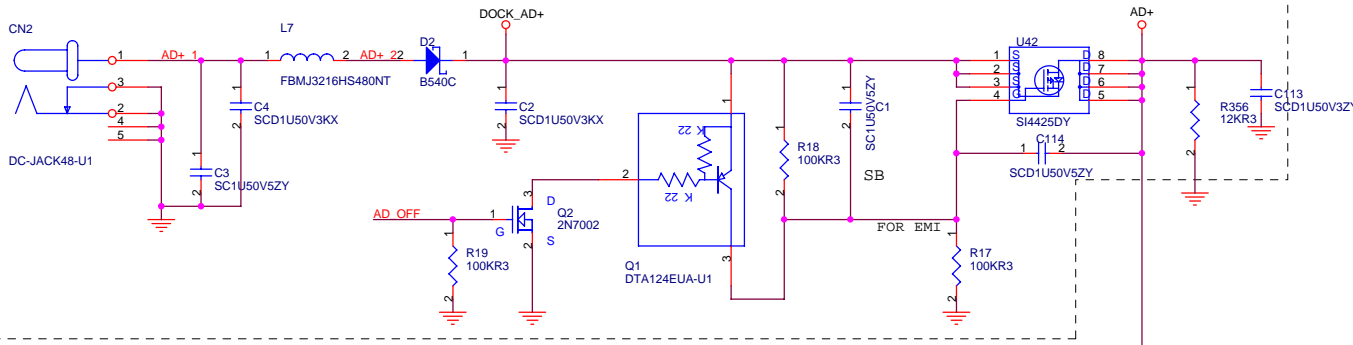


Ton = VCC : 200KHz/300KHz
Ton = GND : 400KHz/500KHz
(5V/3D3V)

SKIP# = VCC : PWM MODE
SKIP# = GND : SKIP MODE
SKIP# = REF/FloatING : Ultrasonic MODE
(25KHz min)

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<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien Z21, Taiwan, R.O.C.</small>	
Title	
MAX1999/3D3V_S5/5V_S5	
Size	Document Number
A3	J2
Date:	Thursday, August 28, 2003
Sheet	36 of 42
Rev	SD

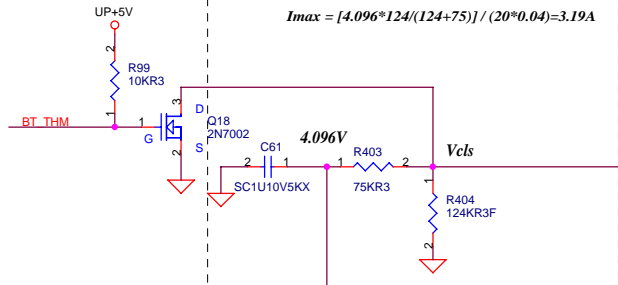
Adaptor In Circuit



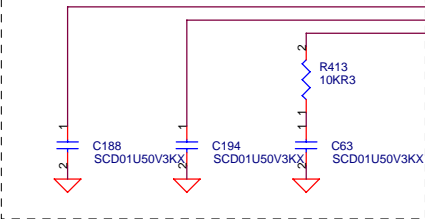
Setting Adaptor Input Current Limit

$$I_{max} = V_{cls} / (20 * R_{sense})$$

$$I_{max} = [4.096 * 124 / (124 + 75)] / (20 * 0.04) = 3.19A$$

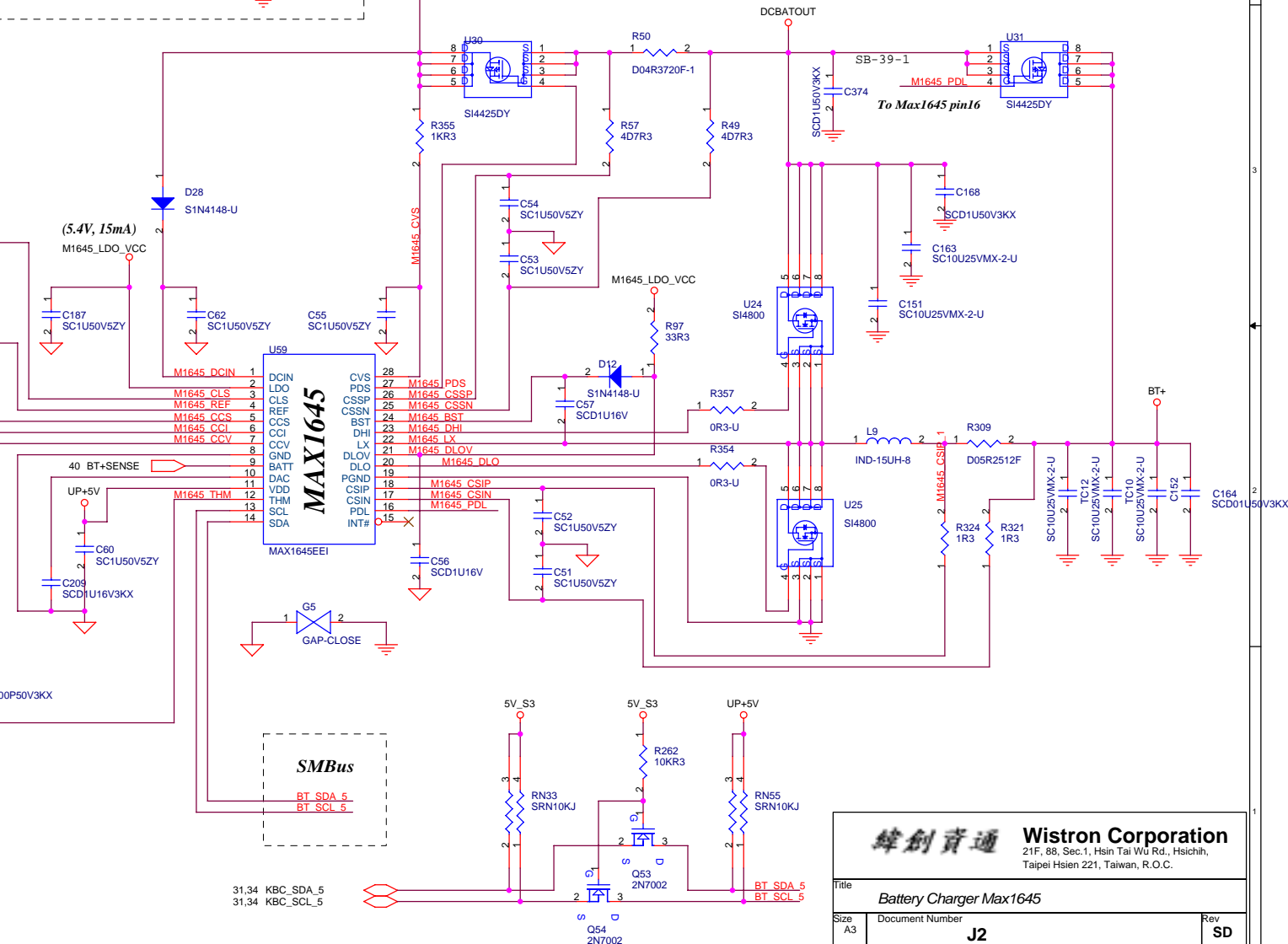


- CCS: Charging Source Compensation Capacitor Connection
- CCI: Battery Current-Loop Compensation Capacitor Connection
- CCV: Battery Voltage-Loop Compensation Capacitor Connection



SMBus

31, 34 KBC_SDA_5
31, 34 KBC_SCL_5

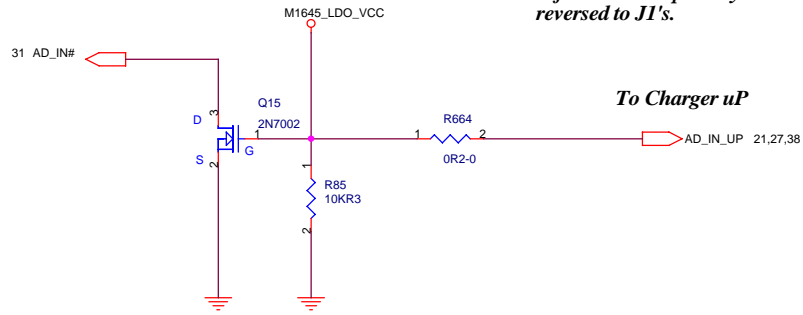


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Title		Battery Charger Max1645	
Size	A3	Document Number	J2
Date:	Thursday, August 28, 2003	Sheet	39 of 42
		Rev	SD

Adaptor In Detection

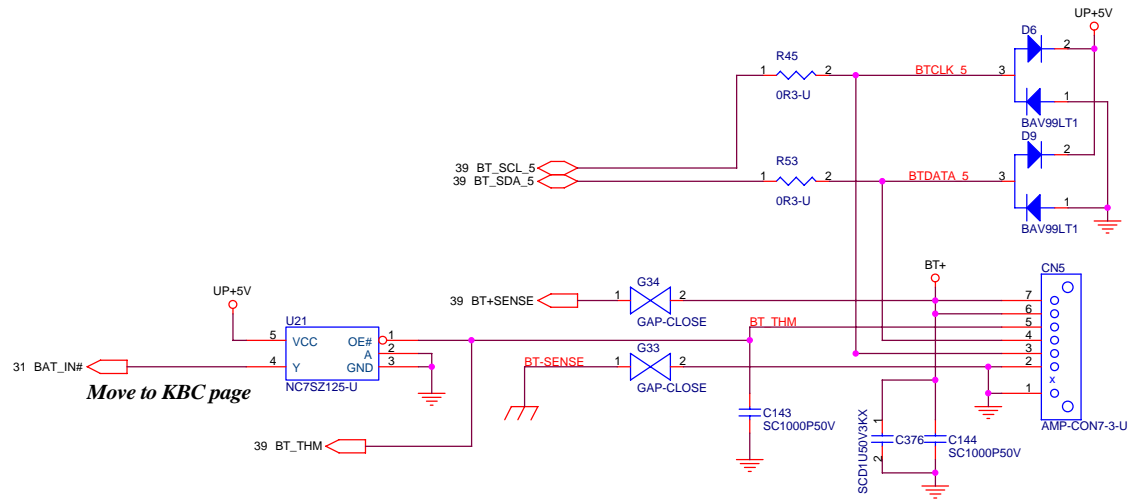
To KBC



Inform SW the polarity is reversed to J1's.

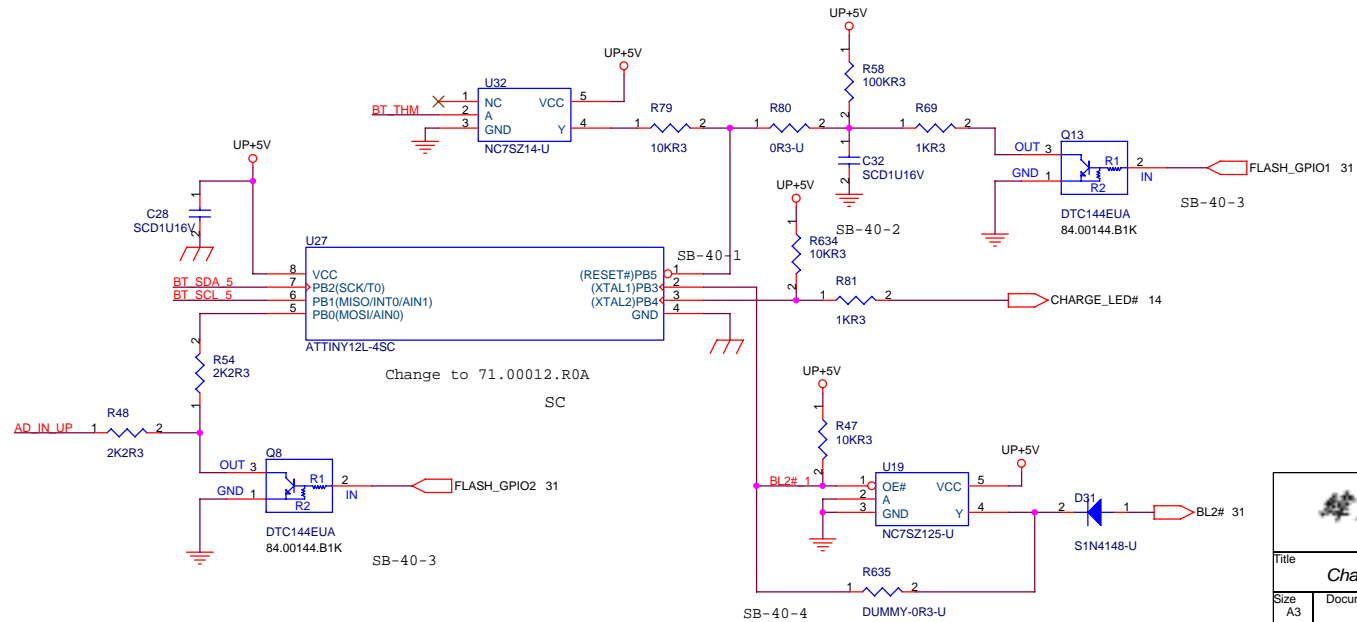
To Charger uP

Battery Conn



Move to KBC page

Charger uP

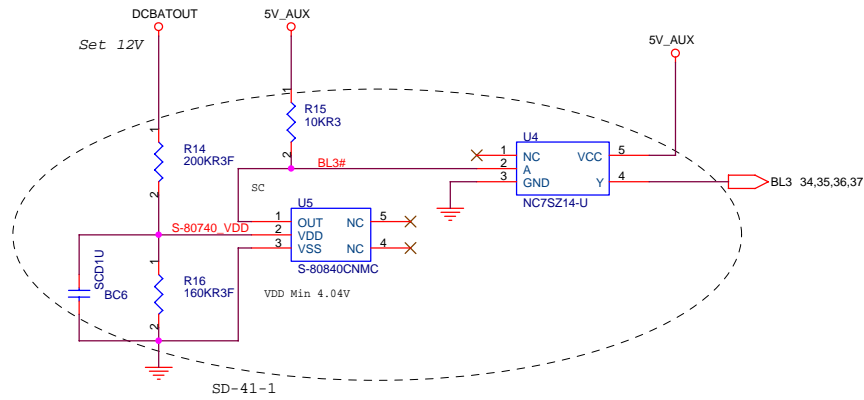


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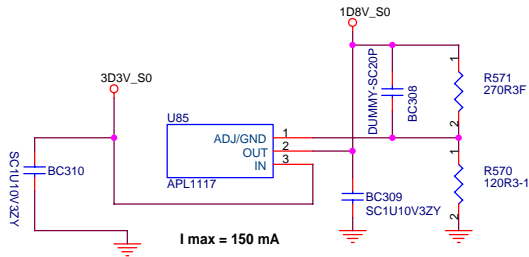
Title: **Charger uP & Battery Conn**

Size A3	Document Number	J2	Rev SD
Date: Wednesday, August 27, 2003	Sheet 40	of 42	

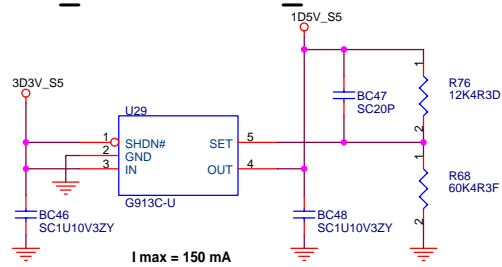
BATTERY LOW3 DETECTOR



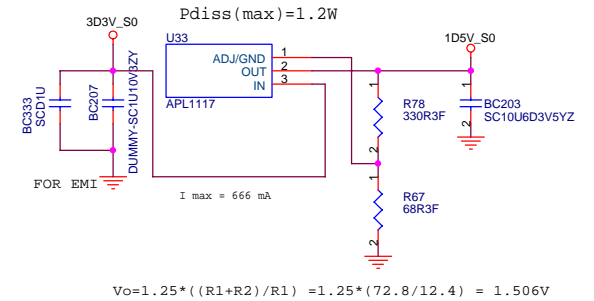
3D3V_S0 --> 1D8V_S0



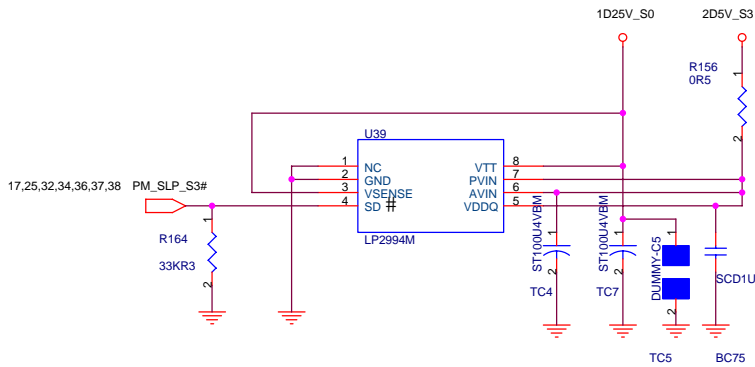
3D3V_S5 --> 1D5V_S5



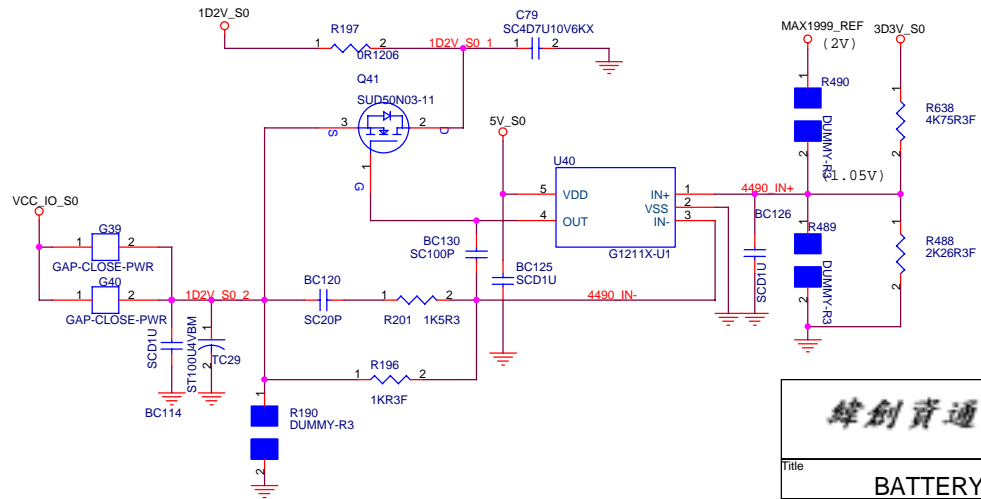
3D3V_S0 -> 1D5V_S0



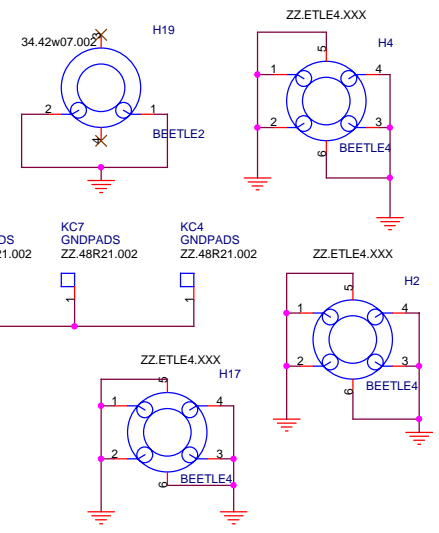
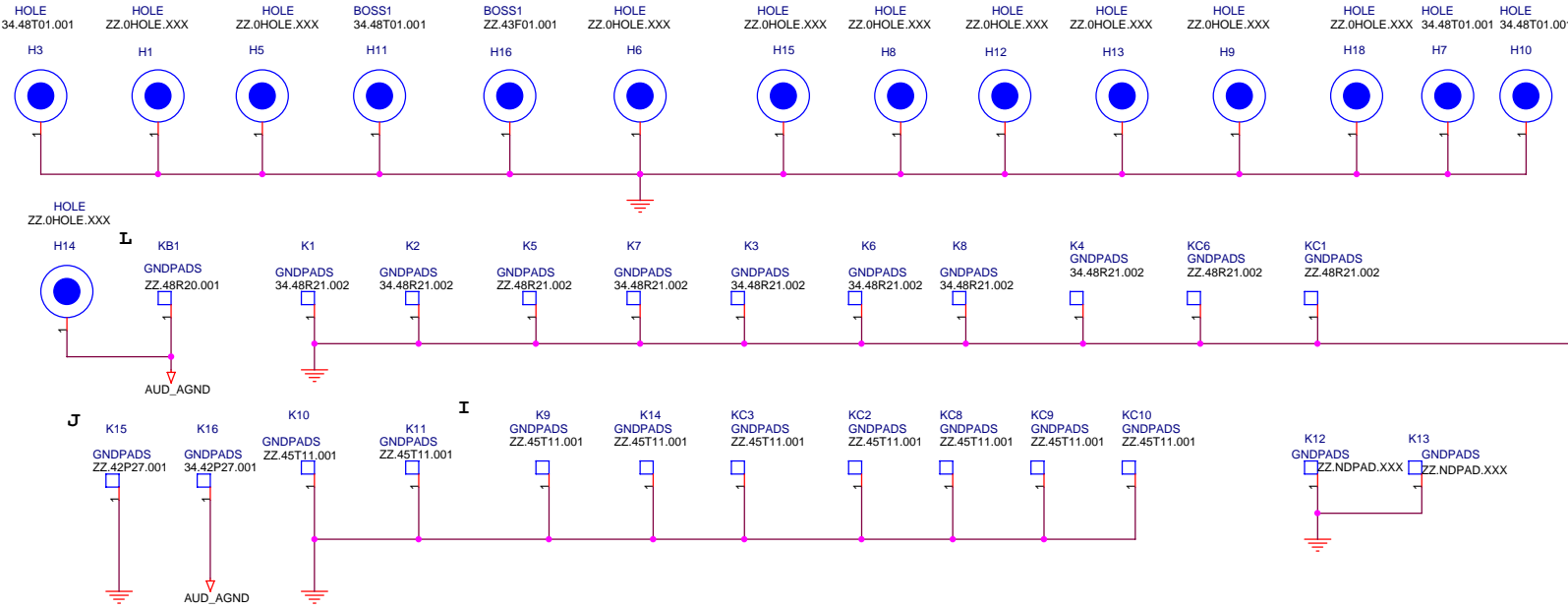
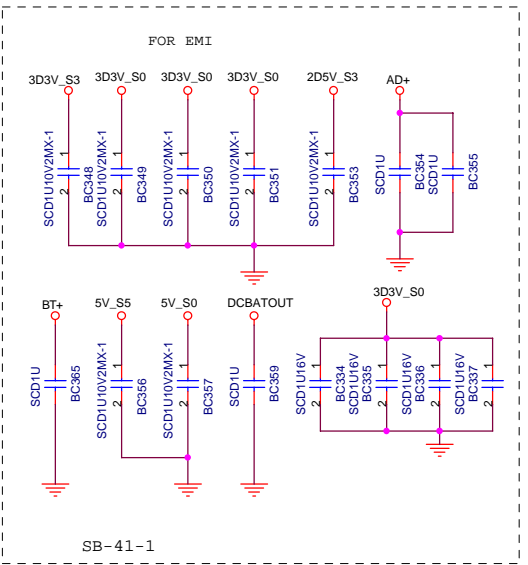
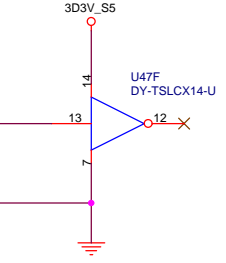
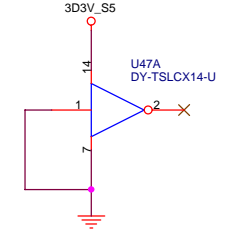
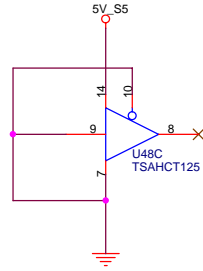
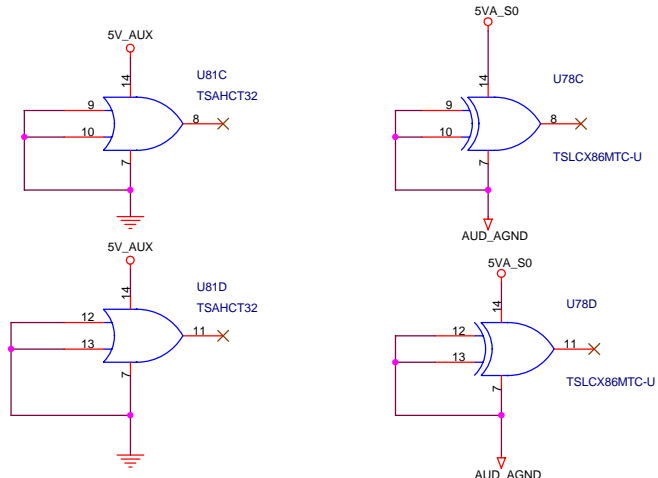
2D5V_S3 -> 1D25V_S0



1D2V_S0 -> VCC_IO_S0 (1.05V)



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Title	
BATTERY/LDO	
Size	Document Number
A3	J2
Date: Thursday, July 17, 2003	Sheet 41 of 42
	Rev SD



緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MISC	
Size A3	Document Number
Date: Friday, August 08, 2003	J2
Sheet 42	of 42
Rev SD	