

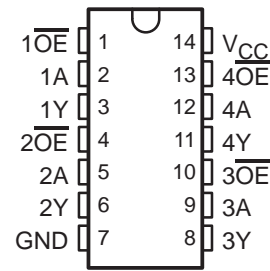
SN74LVT125

3.3-V ABT QUADRUPLE BUS BUFFER WITH 3-STATE OUTPUTS

SCBS133F – MAY 1992 – REVISED OCTOBER 2003

- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} Supports Partial-Power-Down Mode Operation
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

D, DB, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

This bus buffer is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – D | Tube | SN74LVT125D | LVT125 |
| | | Tape and reel | SN74LVT125DR | |
| | SOP – NS | Tape and reel | SN74LVT125NSR | LVT125 |
| | SSOP – DB | Tape and reel | SN74LVT125DBR | LX125 |
| | TSSOP – PW | Tube | SN74LVT125PW | LX125 |
| | | Tape and reel | SN74LVT125PWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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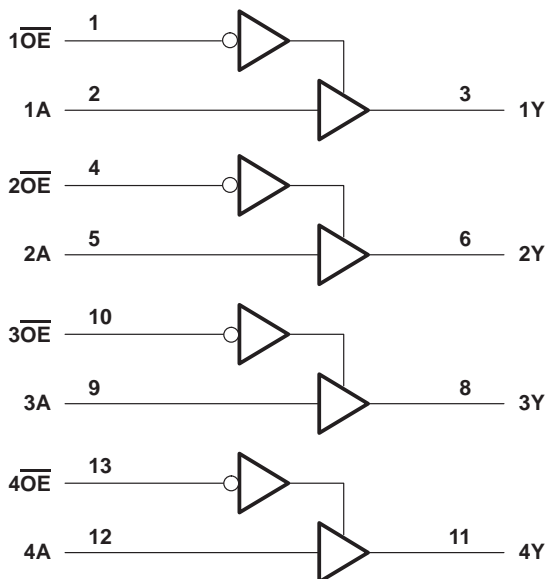
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3.3-V ABT QUADRUPLE BUS BUFFER
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) | -0.5 V to 7 V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_{OH} (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): | |
| D package | 86°C/W |
| DB package | 96°C/W |
| NS package | 76°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----------------|-----|---------|
| V_{CC} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | | 5.5 | V |
| I_{OH} | High-level output current | | -32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|----------------------|---|--|------------------------------------|------|-----------|---------------|
| V_{IK} | $V_{CC} = 2.7\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| V_{OH} | $V_{CC} = \text{MIN to MAX}^\ddagger$, | $I_{OH} = -100\ \mu\text{A}$ | $V_{CC}-0.2$ | | | V |
| | $V_{CC} = 2.7\text{ V}$, | $I_{OH} = -8\text{ mA}$ | 2.4 | | | |
| | $V_{CC} = 3\text{ V}$ | $I_{OH} = -32\text{ mA}$ | 2 | | | |
| V_{OL} | $V_{CC} = 2.7\text{ V}$ | $I_{OL} = 100\ \mu\text{A}$ | | | 0.2 | V |
| | | $I_{OL} = 24\text{ mA}$ | | | 0.5 | |
| | $V_{CC} = 3\text{ V}$ | $I_{OL} = 16\text{ mA}$ | | | 0.4 | |
| | | $I_{OL} = 32\text{ mA}$ | | | 0.5 | |
| | | $I_{OL} = 64\text{ mA}$ | | | 0.55 | |
| I_I | $V_{CC} = 0\text{ or MAX}^\ddagger$, | $V_I = 5.5\text{ V}$ | | | 10 | μA |
| | $V_{CC} = 3.6\text{ V}$ | $V_I = V_{CC}\text{ or GND}$ | Control inputs | | ± 1 | |
| | | $V_I = V_{CC}$ | Data inputs | | | |
| | | $V_I = 0$ | | | -5 | |
| I_{off} | $V_{CC} = 0$, | $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$ | | | ± 100 | μA |
| $I_{I(\text{hold})}$ | $V_{CC} = 3\text{ V}$ | $V_I = 0.8\text{ V}$ | Data inputs | | 75 | μA |
| | | $V_I = 2\text{ V}$ | | | -75 | |
| I_{OZH} | $V_{CC} = 3.6\text{ V}$, | $V_O = 3\text{ V}$ | | | 5 | μA |
| I_{OZL} | $V_{CC} = 3.6\text{ V}$, | $V_O = 0.5\text{ V}$ | | | -5 | μA |
| I_{CC} | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$ | $I_O = 0$, | Outputs high | 0.12 | 0.19 | mA |
| | | | Outputs low | 4.5 | 7 | |
| | | | Outputs disabled | 0.12 | 0.19 | |
| ΔI_{CC}^\S | $V_{CC} = 3\text{ V to }3.6\text{ V}$, | One input at $V_{CC} - 0.6\text{ V}$, | Other inputs at V_{CC} or GND | | 0.2 | mA |
| C_i | $V_I = 3\text{ V or }0$ | | | | 4 | pF |
| C_o | $V_O = 3\text{ V or }0$ | | | | 8 | pF |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



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WITH 3-STATE OUTPUTS

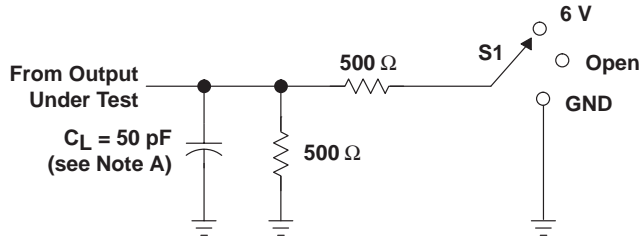
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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|-----------|-----------------|-------------|--|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1 | 2.7 | 4 | 4.5 | | ns |
| t_{PHL} | | | 1 | 2.9 | 3.9 | 4.9 | | |
| t_{PZH} | \overline{OE} | Y | 1 | 3.4 | 4.7 | 6 | | ns |
| t_{PZL} | | | 1.1 | 3.4 | 4.7 | 6.5 | | |
| t_{PHZ} | \overline{OE} | Y | 1.8 | 3.7 | 5.1 | 5.7 | | ns |
| t_{PLZ} | | | 1.3 | 2.6 | 4.5 | 4 | | |

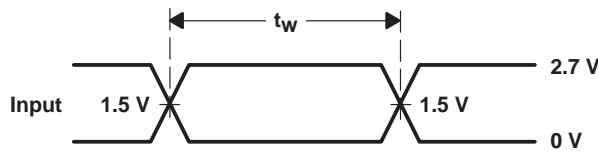
† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

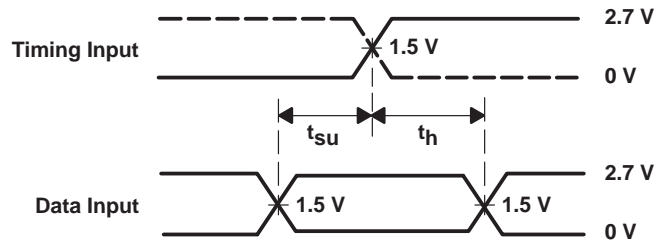


| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |

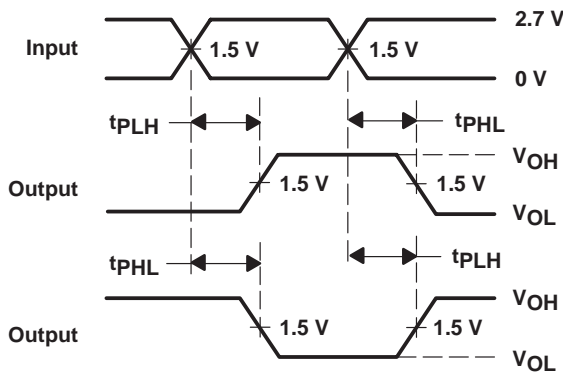
LOAD CIRCUIT FOR OUTPUTS



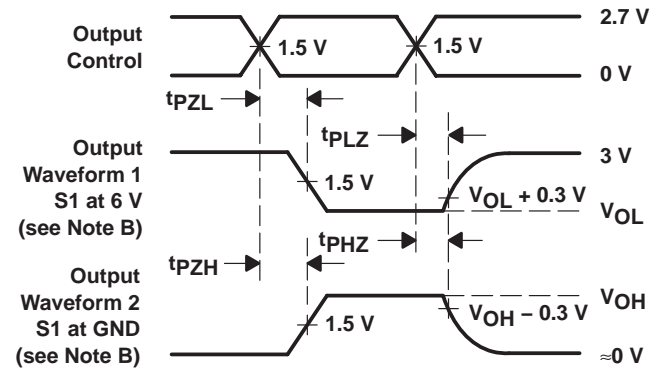
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|----------------------------------|
| SN74LVT125D | NRND | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125DBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI | Replaced by SN74LVT125DBR |
| SN74LVT125DBR | NRND | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125DBRG4 | NRND | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125DG4 | NRND | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74LVT125DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74LVT125NSR | NRND | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125PW | NRND | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125PWG4 | NRND | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Samples Not Available |
| SN74LVT125PWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | Replaced by SN74LVT125PWR |
| SN74LVT125PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74LVT125PWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVT125 :

- Automotive: [SN74LVT125-Q1](#)
- Enhanced Product: [SN74LVT125-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVT125DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVT125DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVT125DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVT125NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVT125PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

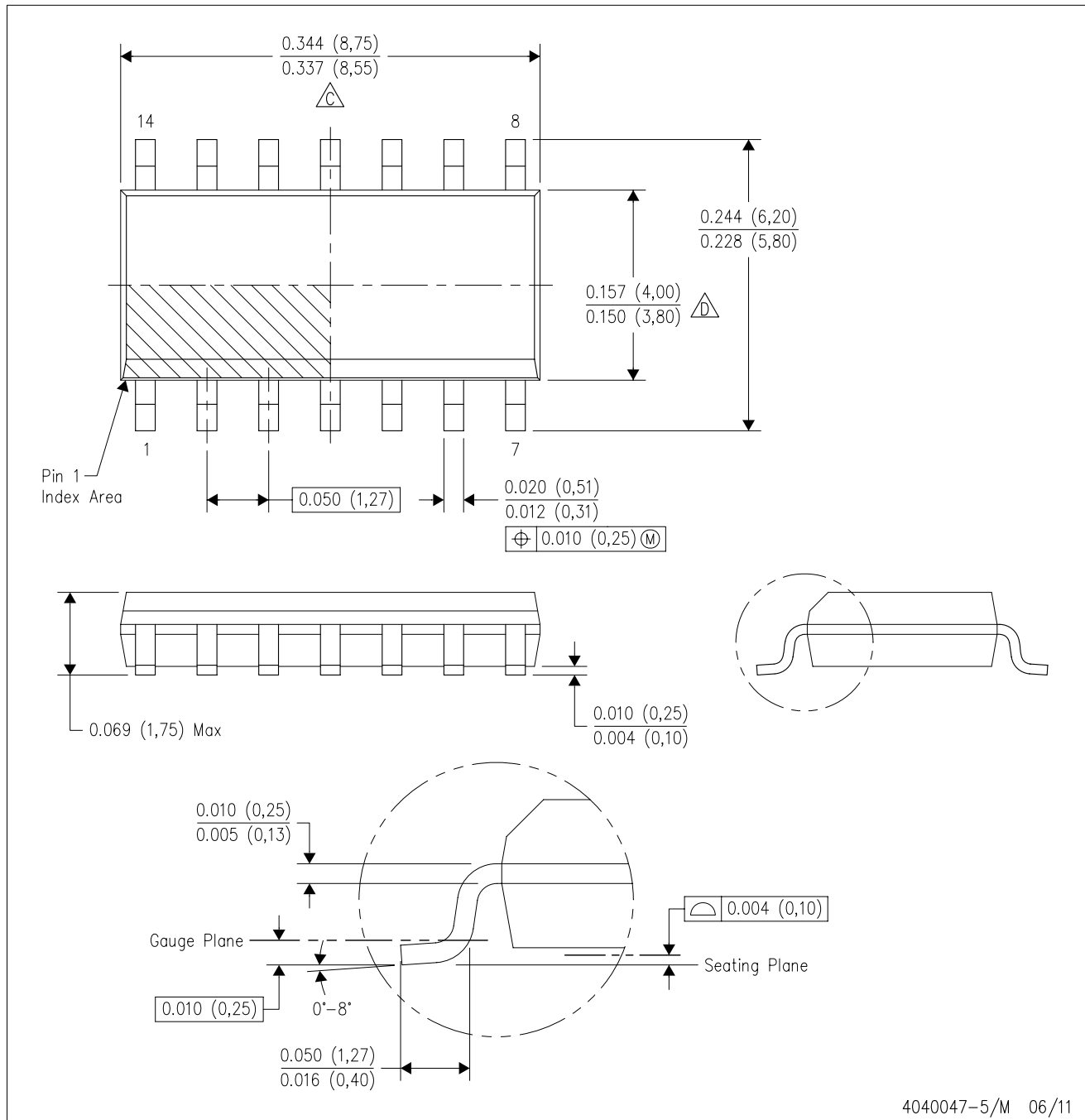
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVT125DBR | SSOP | DB | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVT125DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVT125DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74LVT125NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVT125PWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

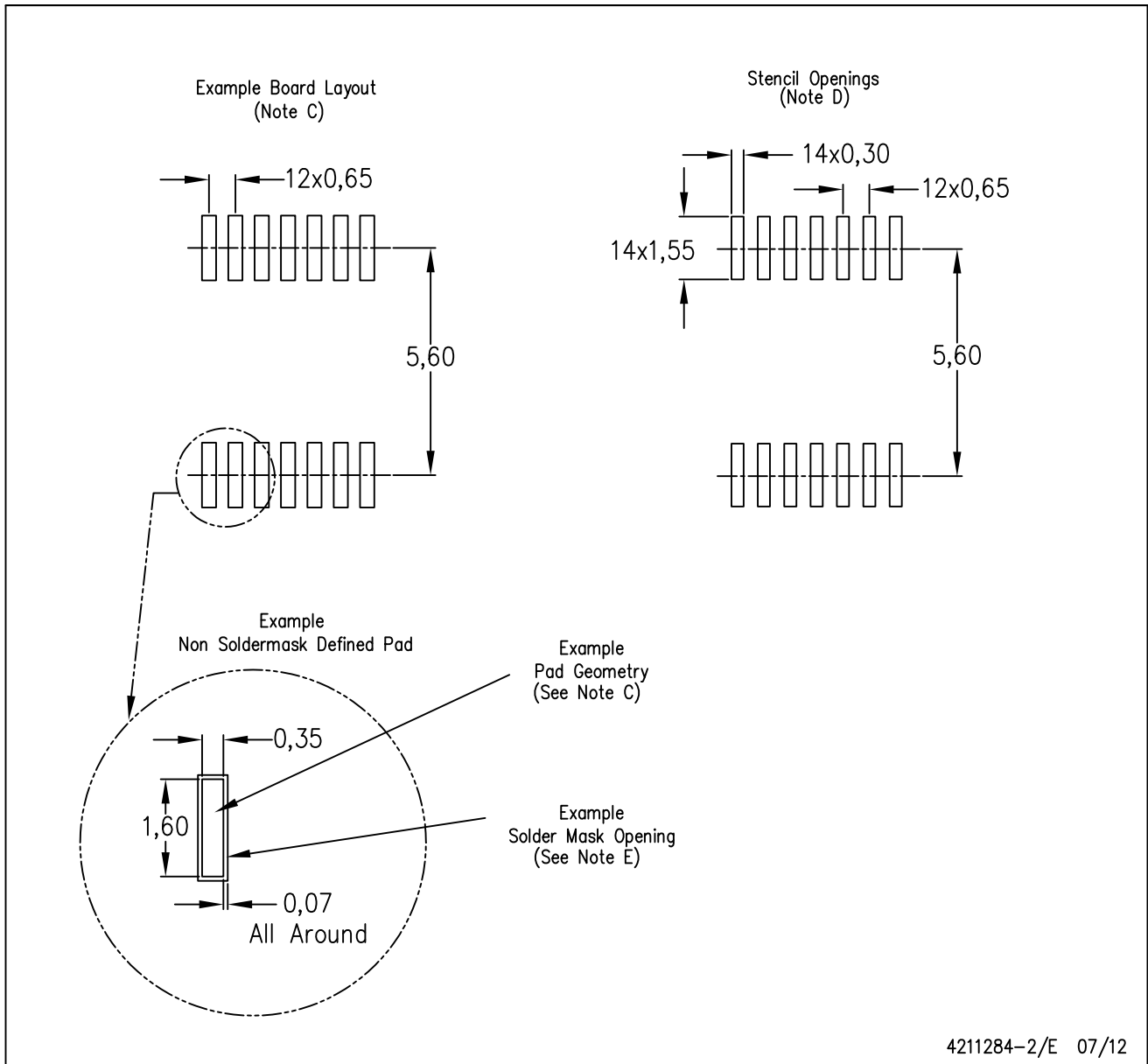


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/E 07/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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