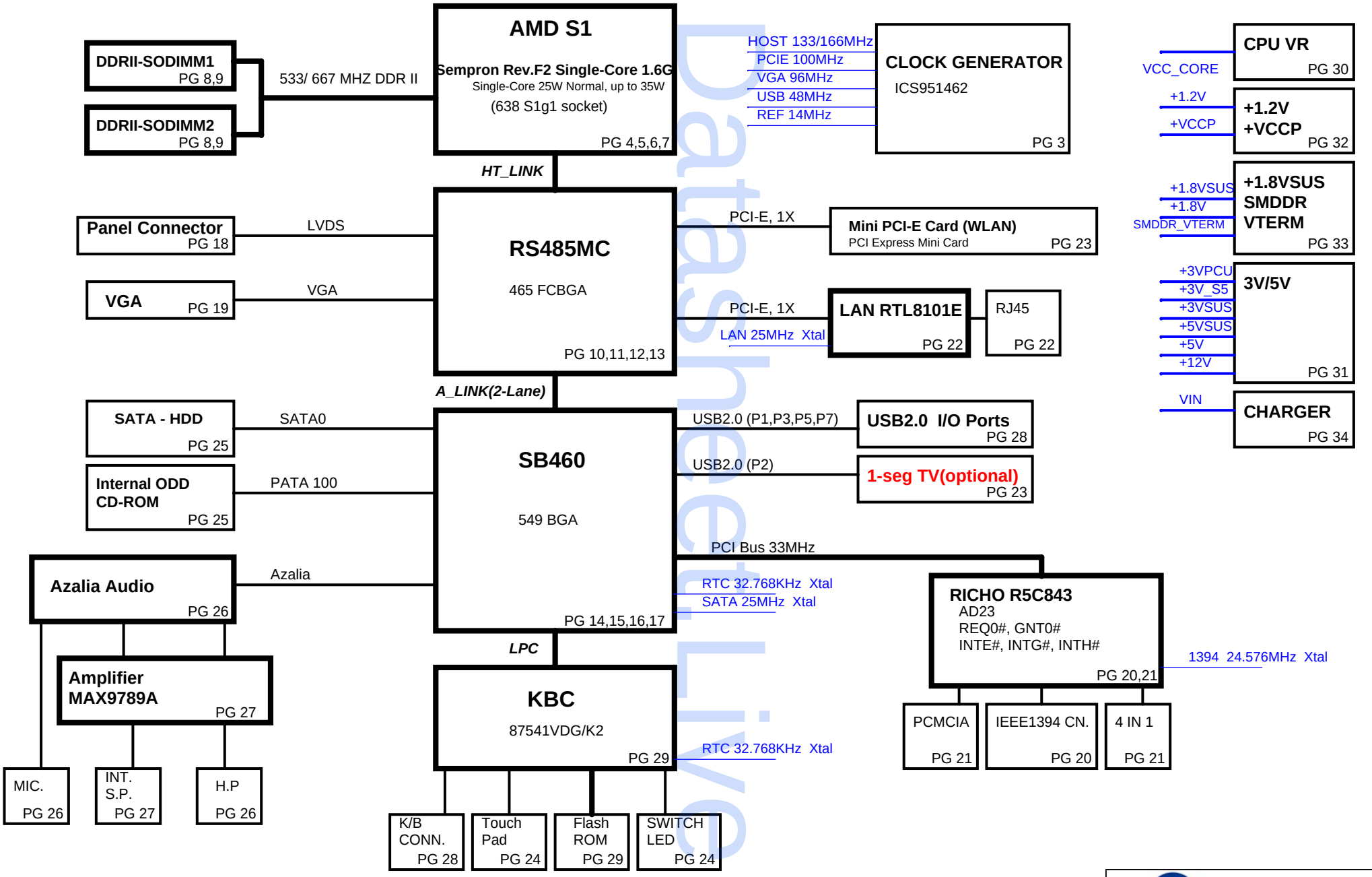
ES2 BLOCK DIAGRAM



Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: Block Diagram	Rev D
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Page 01: Block diagram
Page 02: System information
Page 03: Clock generator ICS951462
Page 04: AMD S1 HT
Page 05: AMD S1 DDR2
Page 06: AMD S1 control&debug
Page 07: AMD S1 power
Page 08: DDR2 SODIMM X 2
Page 09: DDR2 Termination
Page 10: RS485M HT interface
Page 11: RS485M PCIE interface
Page 12: RS485M Sytem I/F & Clock Gen.
Page 13: RS485M Power
Page 14: SB460 PCIE/PCI/RTC/LPC/CPU/XTAL Interface
Page 15: SB460 USB/ACPI/AZALIA/AC 97 Interface
Page 16: SB460 SATA/PATA/HW Monitor/Power Interface
Page 17: SB460 Straps
Page 18: LCD PANEL
Page 19: CRT
Page 20: R5C843 PCI/1394 Interface
Page 21: R5C843 PCMCIA/4 IN 1 Interface
Page 22: PCI LAN RTL8101E/RJ45
Page 23: FAN / MINI PCIE / 1-seg TV
Page 24: LEDs / TP CONNECTOR
Page 25: SATA HDD/PATA ODD Connector
Page 26: CODEC ALC262 Mic/HP
Page 27: Audio Amplifier MAX9789A
Page 28: USB Connector/KeyBoard Connector
Page 29: KBC PC87541/BIOS ROM
Page 30: CPU CORE MAX8774
Page 31: 3V/5V MAX8734
Page 32: 1.2V SC470/1.5V/1.2V
Page 33: 1.8V/0.9V TPS51116
Page 34: Battery Charger MAX8724
Page 35: Battery Connector

Voltage Rails

Power	Voltage	ON S0~S2	ON S3	ON S4	ON S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
RVCC3	3V	V	V	V		RVCC_ON
RVCC1.8	1.8V	V	V	V		RVCC_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VLDT_RUN	1.2V	V				VLDT_ON

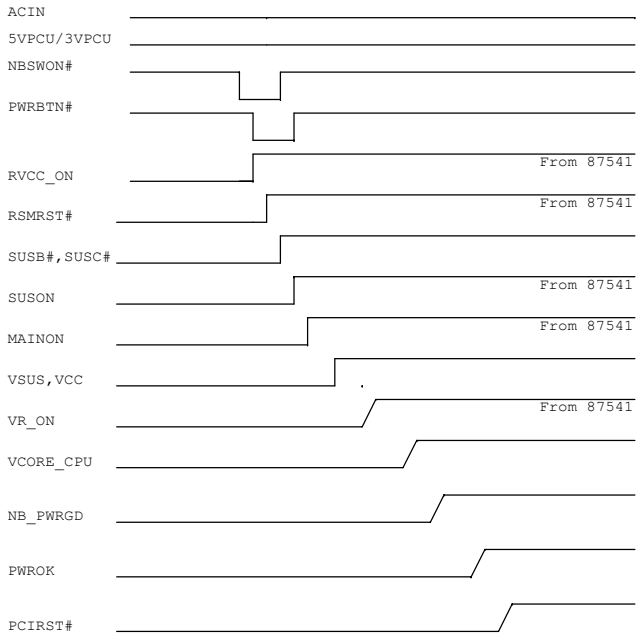
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

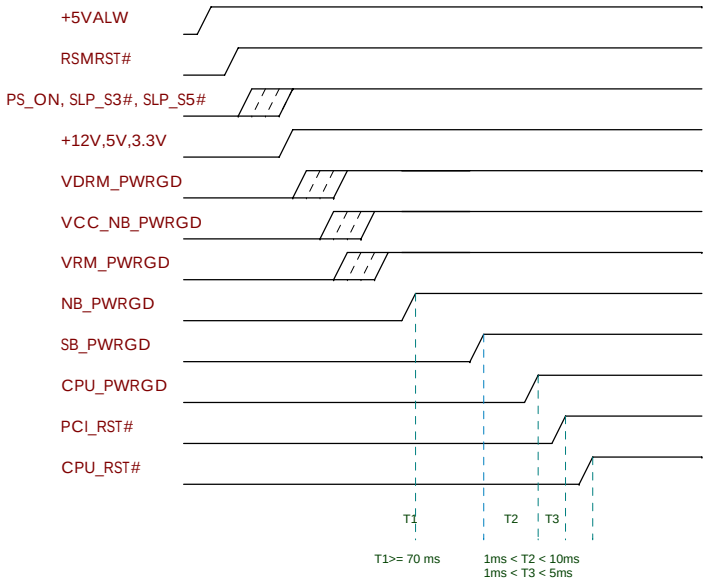
PCI DEVICES IRQ ROUTING

ES2 PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
R5C843	AD23	REQ0# / GNT0#	INT E/F/G

Power On Sequence

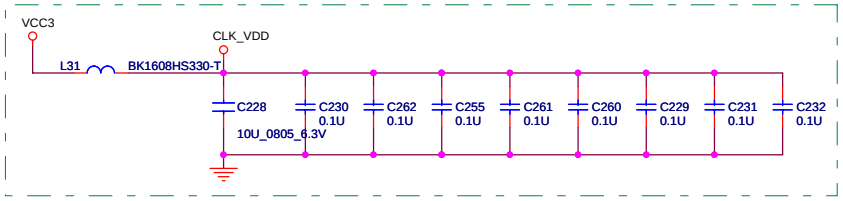


BONEFISH POWER UP SEQUENCE

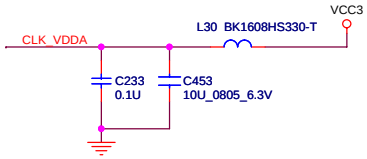


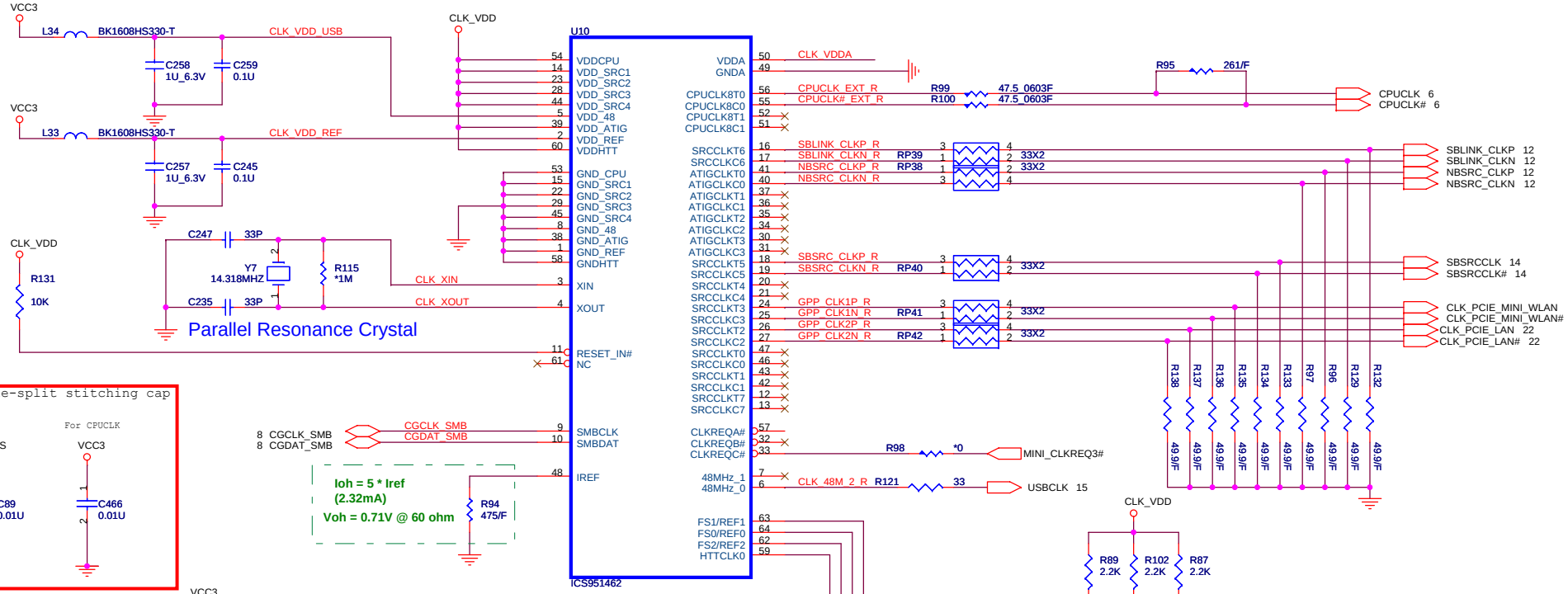
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	System information	D
Date: Thursday, May 24, 2007	Sheet 2 of 35	



Put Decoupling Caps close to Clock Fen. power pin






```
CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2
```

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	CLOCK GENERATOR ICS951462	D
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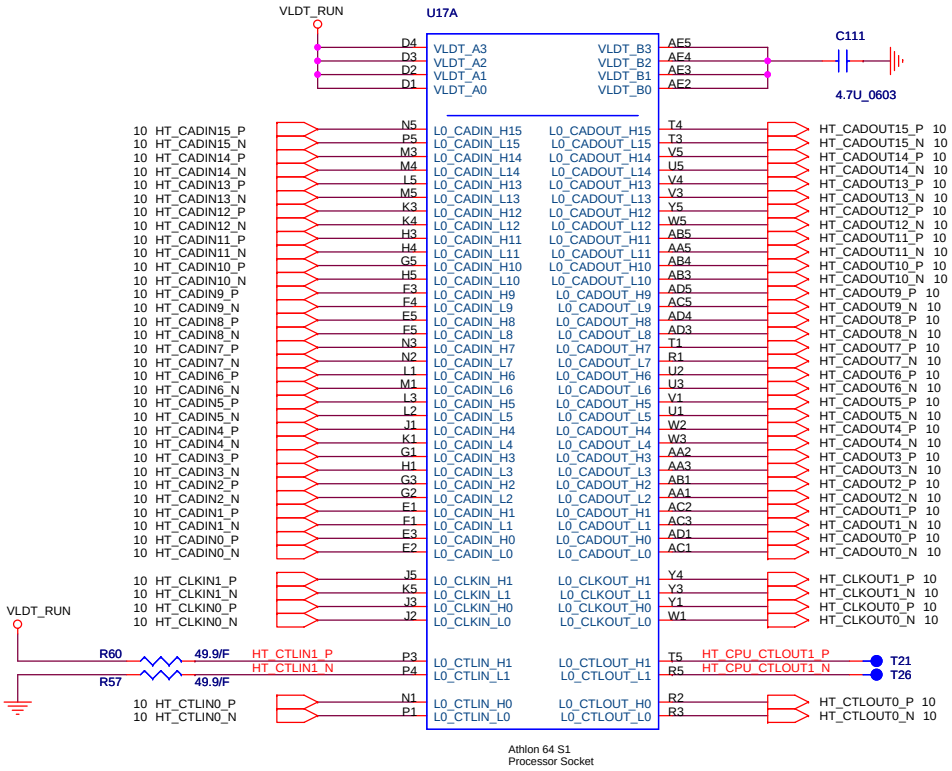

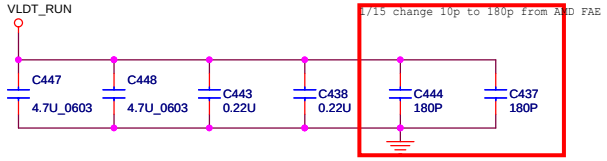

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: ATHLON64 HT I/F	Rev: D
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Processor DDR2 Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"

1.8VSUS

R59 2K/F

CPU_M_VREF

C134 0.1U

C140 1000P_16V

R54 2K/F

R215 39.2F

R214 39.2F

T16

SMDDR_VTERM

U17B

W17 MEMVREF

VTT_SENSE Y10 VTT_SENSE

M_ZN AE10 MEMZN

M_ZP AE10 MEMZP

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

8,9 M_A_CS#3 V19 MA0_CS_L3
8,9 M_A_CS#2 J22 MA0_CS_L2
8,9 M_A_CS#1 V22 MA0_CS_L1
8,9 M_A_CS#0 T19 MA0_CS_L0

MA0_CLK_H2 Y16 M_CLKOUT1 8
MA0_CLK_L2 AA16 M_CLKOUT1# 8
MA0_CLK_H1 E16 M_CLKOUT0 8
MA0_CLK_L1 F16 M_CLKOUT0# 8

8,9 M_B_CS#3 Y26 MB0_CS_L3
8,9 M_B_CS#2 J24 MB0_CS_L2
8,9 M_B_CS#1 W24 MB0_CS_L1
8,9 M_B_CS#0 U23 MB0_CS_L0

MB0_CLK_H2 AF18 M_CLKOUT4 8
MB0_CLK_L2 AF17 M_CLKOUT4# 8
MB0_CLK_H1 A17 M_CLKOUT3 8
MB0_CLK_L1 A18 M_CLKOUT3# 8

8,9 M_CKE3 H26 MB_CKE1
8,9 M_CKE2 J23 MB_CKE0
8,9 M_CKE1 J20 MA_CKE1
8,9 M_CKE0 J21 MA_CKE0

MB0_ODT1 W23 M_ODT3 8,9
MB0_ODT0 W26 M_ODT2 8,9
MA0_ODT1 V20 M_ODT1 8,9
MA0_ODT0 U19 M_ODT0 8,9

8,9 M_A_A[0..15] M_B_A[0..15] 8,9

M_A_A15 K19 MA_ADD15 — MB_ADD15 J25 M_B_A15
M_A_A14 K20 MA_ADD14 — MB_ADD14 J26 M_B_A14
M_A_A13 V24 MA_ADD13 — MB_ADD13 W25 M_B_A13
M_A_A12 K24 MA_ADD12 — MB_ADD12 L23 M_B_A12
M_A_A11 L20 MA_ADD11 — MB_ADD11 L25 M_B_A11
M_A_A10 R19 MA_ADD10 — MB_ADD10 U25 M_B_A10
M_A_A9 L19 MA_ADD9 — MB_ADD9 L24 M_B_A9
M_A_A8 L22 MA_ADD8 — MB_ADD8 M26 M_B_A8
M_A_A7 L21 MA_ADD7 — MB_ADD7 L26 M_B_A7
M_A_A6 M19 MA_ADD6 — MB_ADD6 N23 M_B_A6
M_A_A5 M20 MA_ADD5 — MB_ADD5 N24 M_B_A5
M_A_A4 M24 MA_ADD4 — MB_ADD4 N25 M_B_A4
M_A_A3 M22 MA_ADD3 — MB_ADD3 N26 M_B_A3
M_A_A2 N22 MA_ADD2 — MB_ADD2 P24 M_B_A2
M_A_A1 N21 MA_ADD1 — MB_ADD1 P26 M_B_A1
M_A_A0 R21 MA_ADD0 — MB_ADD0 T24 M_B_A0

8,9 M_A_BS#2 K22 MA_BANK2 — MB_BANK2 K26 M_B_BS#2 8,9
8,9 M_A_BS#1 R20 MA_BANK1 — MB_BANK1 T26 M_B_BS#1 8,9
8,9 M_A_BS#0 T22 MA_BANK0 — MB_BANK0 U26 M_B_BS#0 8,9

8,9 M_A_RAS# T20 MA_RAS_L — MB_RAS_L U24 M_B_RAS# 8,9
8,9 M_A_CAS# U20 MA_CAS_L — MB_CAS_L V26 M_B_CAS# 8,9
8,9 M_A_WE# U21 MA_WE_L — MB_WE_L U22 M_B_WE# 8,9

DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

To SODIMM socket B (Far)

To SODIMM socket A (near)

U17C

8 M_B_DQ[0..63] — M_B_DQ63 AD11 … M_B_DQ0 C11 — MB_DATA63 … MB_DATA0 — MA_DATA63 … MA_DATA0 — M_A_DQ63 … M_A_DQ0 — M_A_DQ[0..63] 8

8 M_B_DM[0..7] — M_B_DM7 AD12 … M_B_DM0 A12 — MB_DM7 … MB_DM0 — MA_DM7 … MA_DM0 — M_A_DM7 … M_A_DM0 — M_A_DM[0..7] 8

8 M_B_DQS[0..7] — M_B_DQS0 AE12 … M_B_DQS7 B12 — MB_DQS_H7 … MB_DQS_L0 — MA_DQS_H7 … MA_DQS_L0 — M_A_DQS7 … M_A_DQS0 — M_A_DQS[0..7] 8

8 M_B_DQS#[0..7] — M_B_DQS#0 F26 … M_B_DQS#7 AE12 — M_A_DQS#7 … M_A_DQS#0 — M_A_DQS#[0..7] 8

DDR: DATA
Athlon 64 S1
Processor Socket

SMDDR_VTERM

C74 4.7U_0603 — C450 4.7U_0603 — C72 4.7U_0603 — C77 4.7U_0603 — C445 0.22U — C429 0.22U — C81 0.22U — C446 0.22U — C73 1000P_16V — C430 1000P_16V — C440 1000P_16V — C439 1000P_16V — C83 180P — C449 180P — C78 180P — C75 180P

Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	ATHLON64 DDRII MEMORY I/F	D

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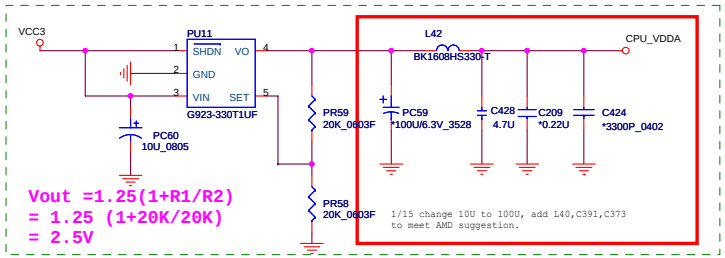
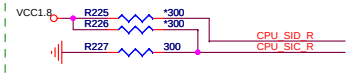
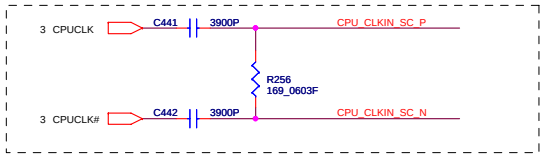
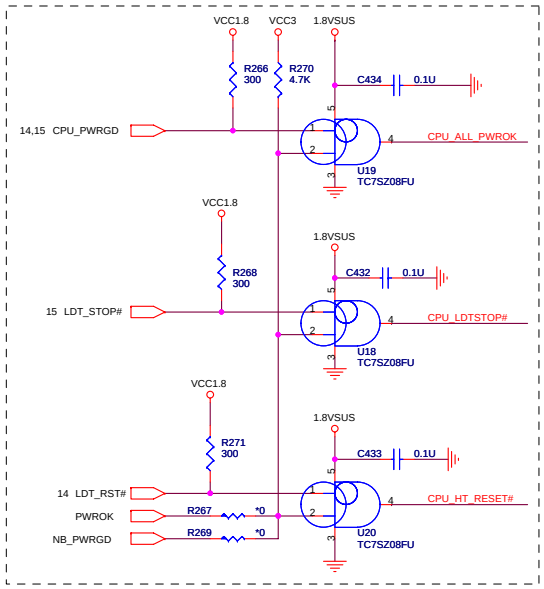
ATHLON Control and Debug

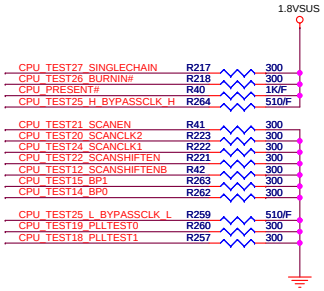


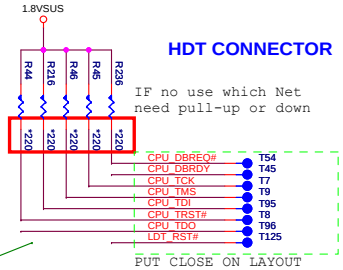
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.







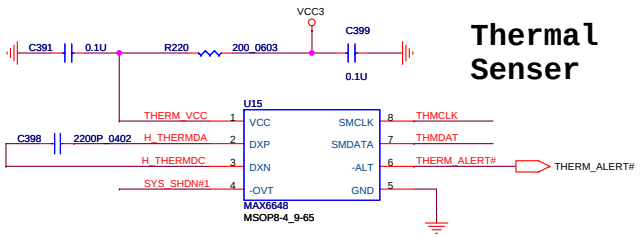


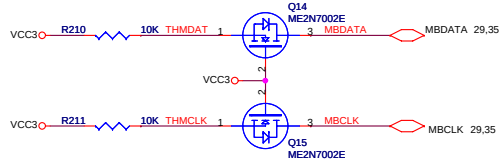


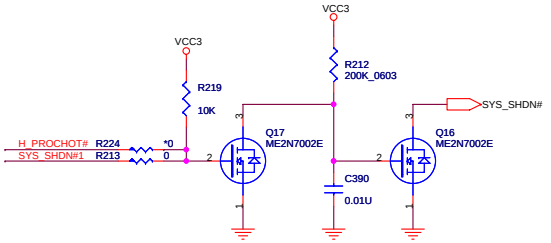
HDT CONNECTOR

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

Thermal Senser







Quanta Computer Inc.	PROJECT : ES2	
Size	Document Number: ATHLON64 CTRL & DEBUG	Rev: D
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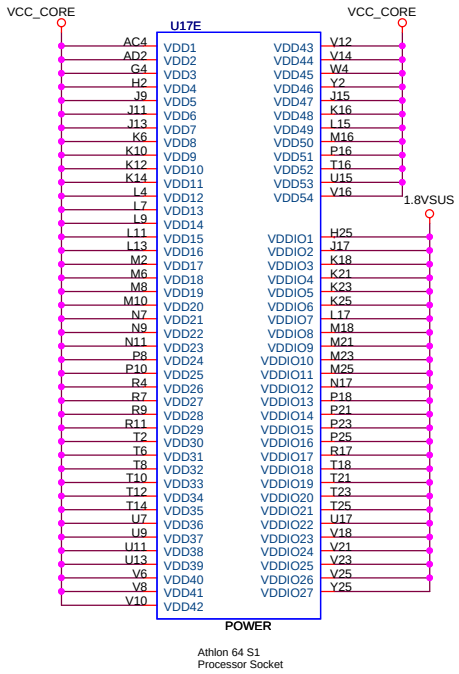
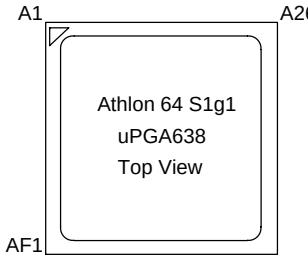
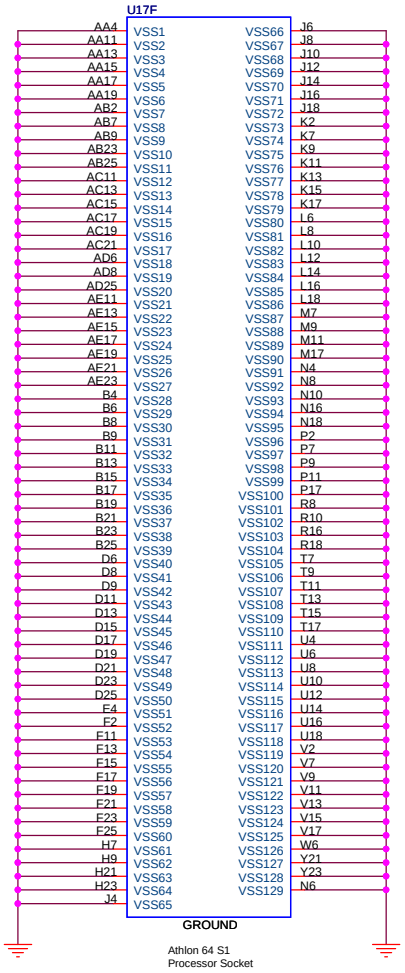
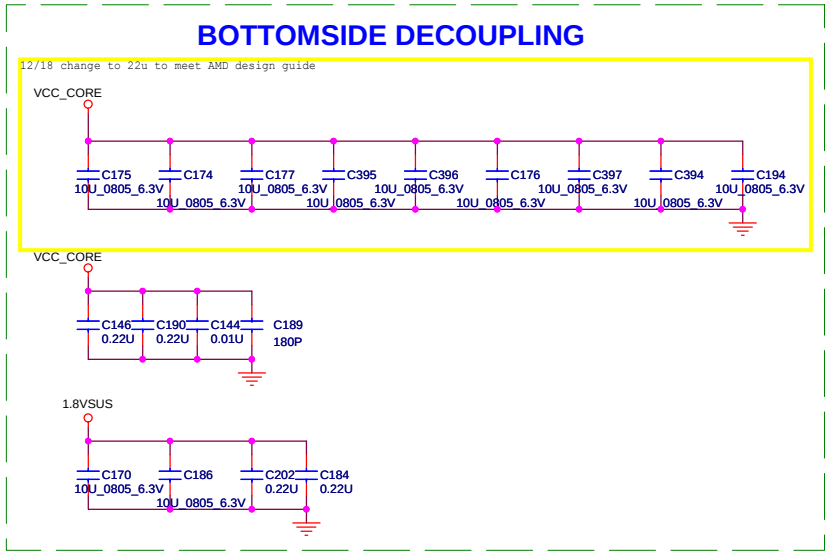
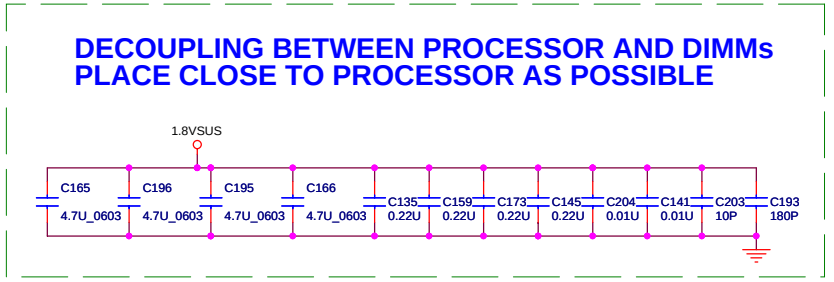
PROCESSOR POWER AND GROUND

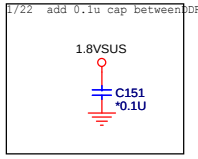












Turion64 X2 TL-50 Rev.F2 (TMDTL50HAX4CT) AJDTL50VG26

Sempron-64 Single core Rev.F2 (SMS3200HAX4CM) AJ03200VG11

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: ATHLON64 PWR & GND	Rev: D
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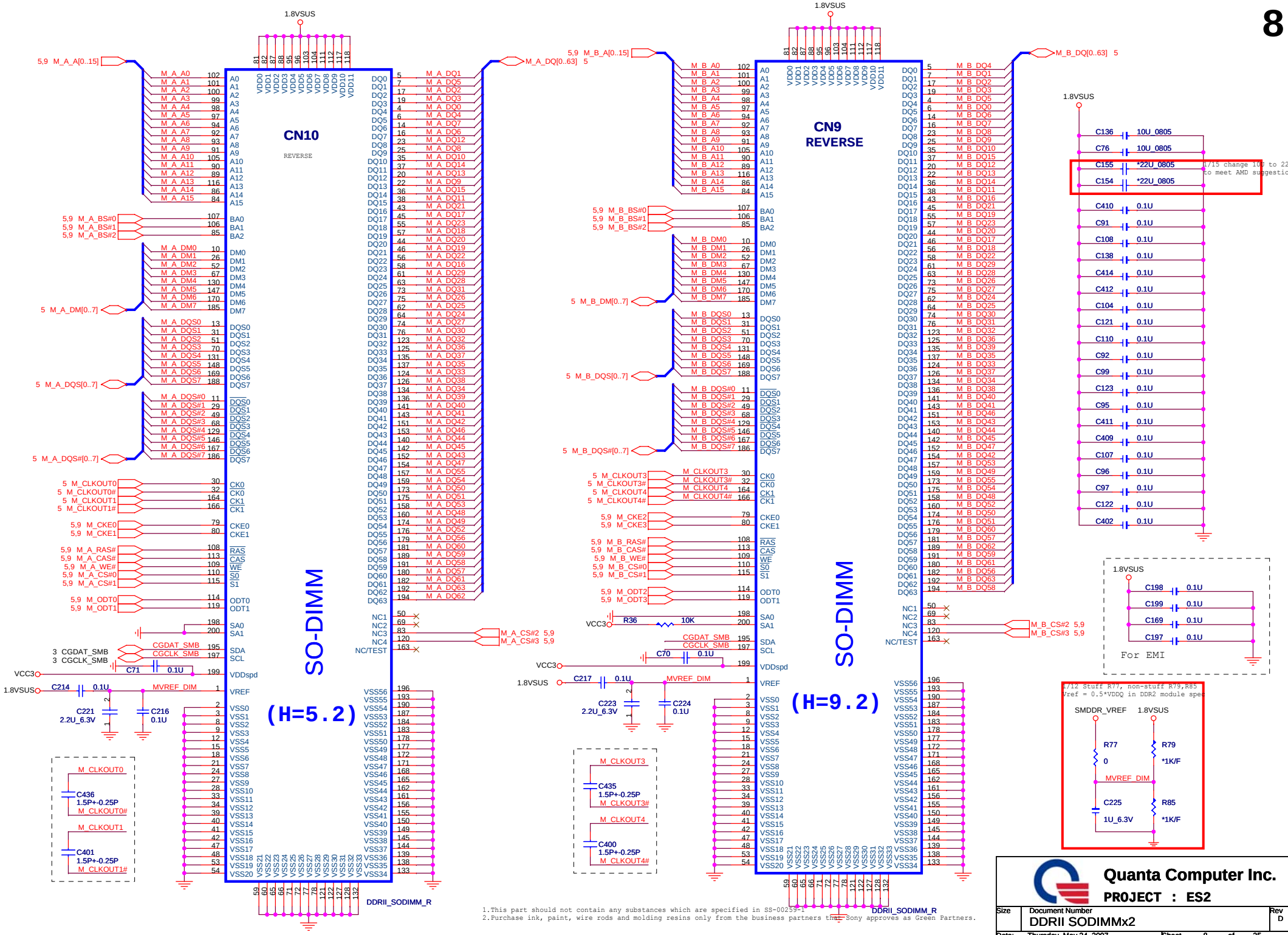
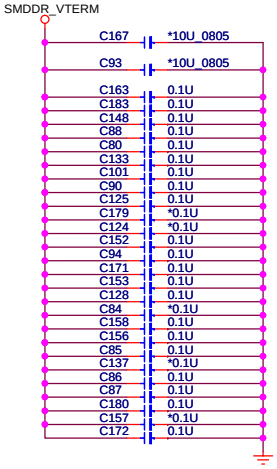


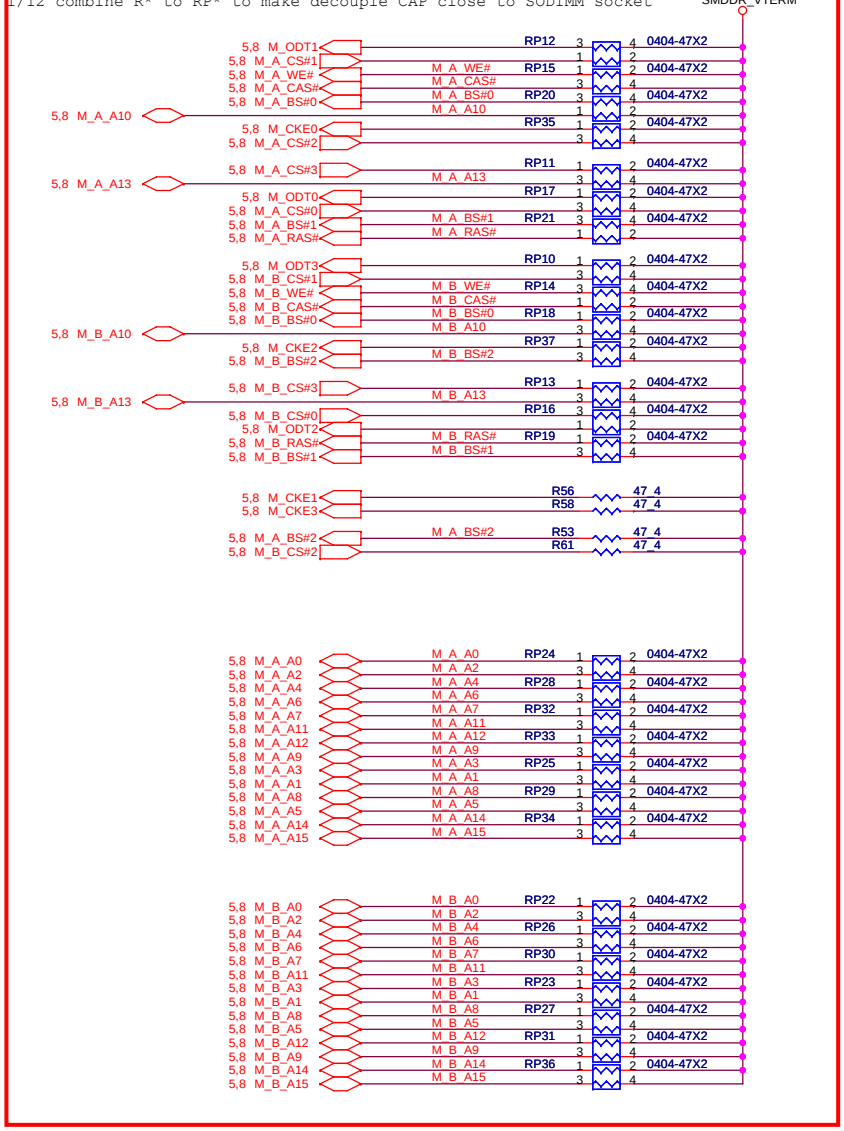
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: DDRII SODIMMx2	Rev: D
Date: Thursday, May 24, 2007	Sheet 8 of 35	



1/22 there is no layout space for decouple cap between 1.8VSUS and SMDDR_VTERM.

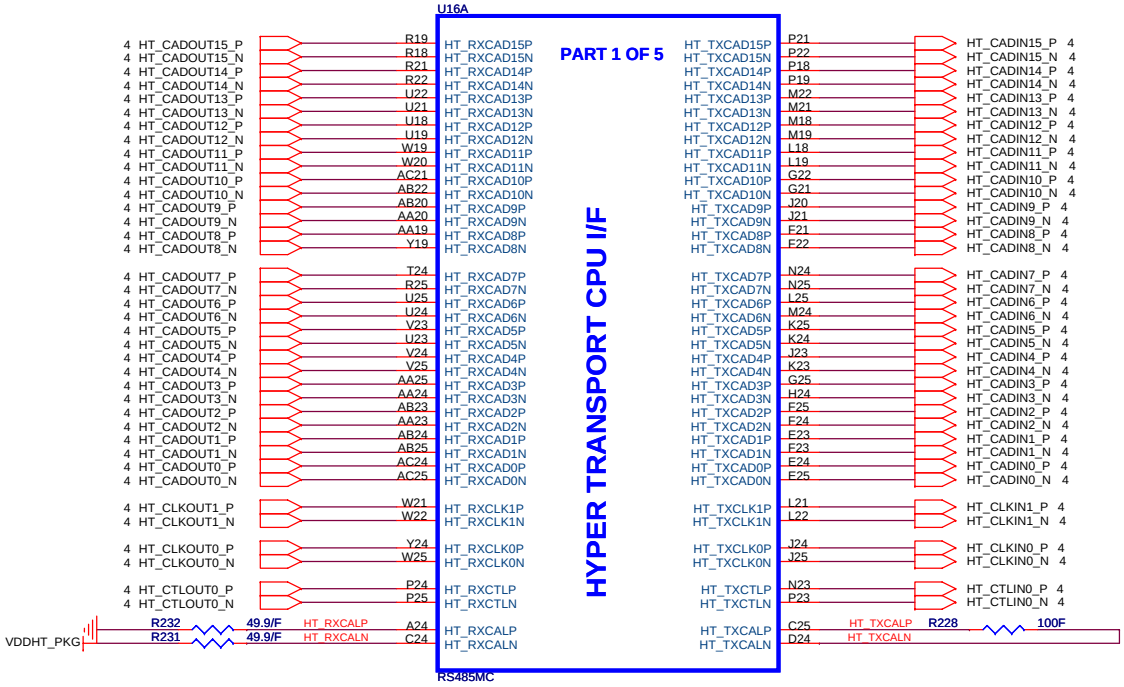
1/12 combine R* to RP* to make decouple CAP close to SODIMM socket



Quanta Computer Inc.

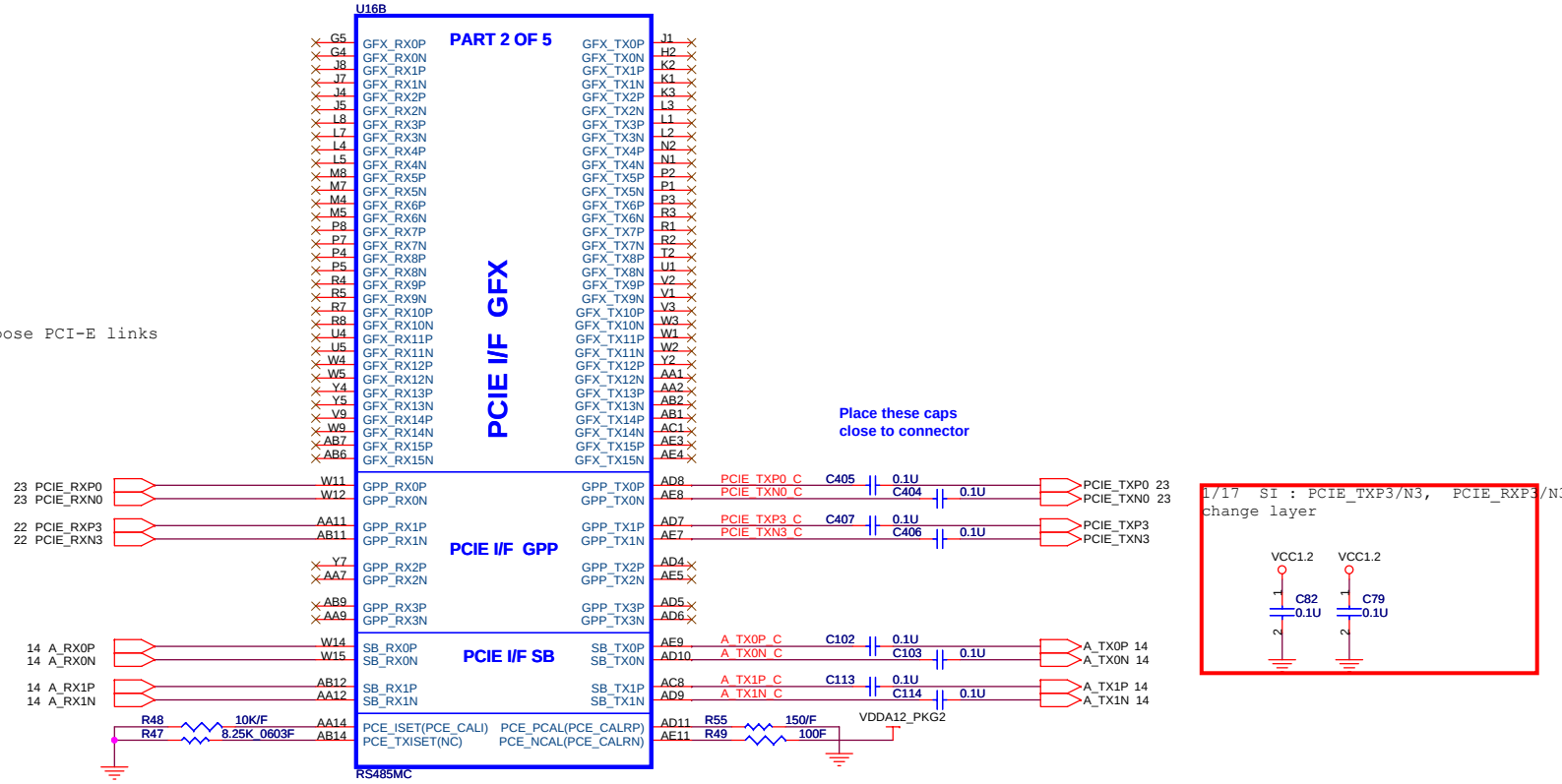
PROJECT : ES2

Size	Document Number	Rev
	DDRII TERMINATION	D
Date: Thursday, May 24, 2007	Sheet 9 of 35	

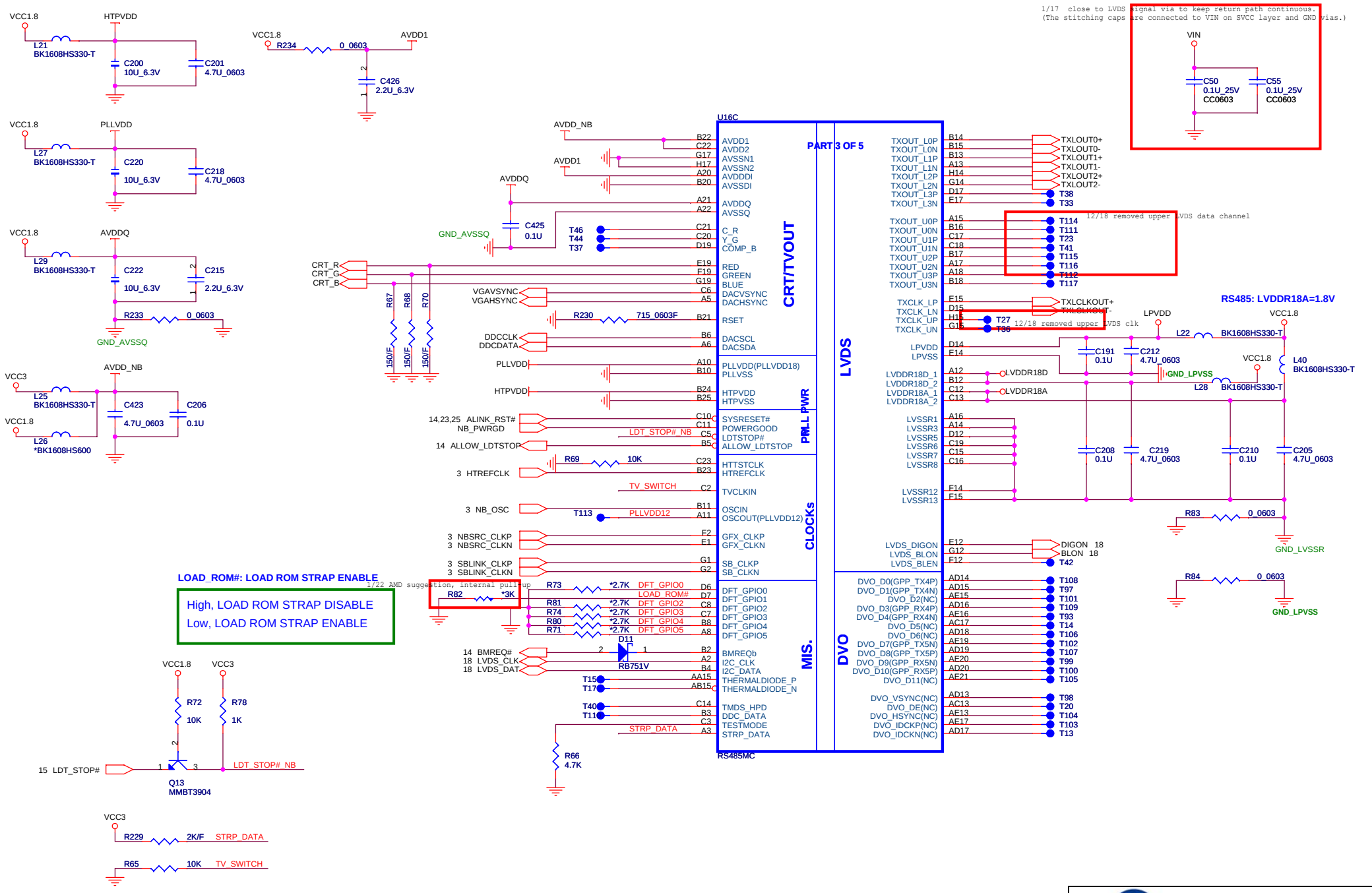


Quanta Computer Inc.	
PROJECT : ES2	
Size	Document Number: RS485MC HT LINK0 I/F — Rev: D
Date: Thursday, May 24, 2007	Sheet 10 of 35

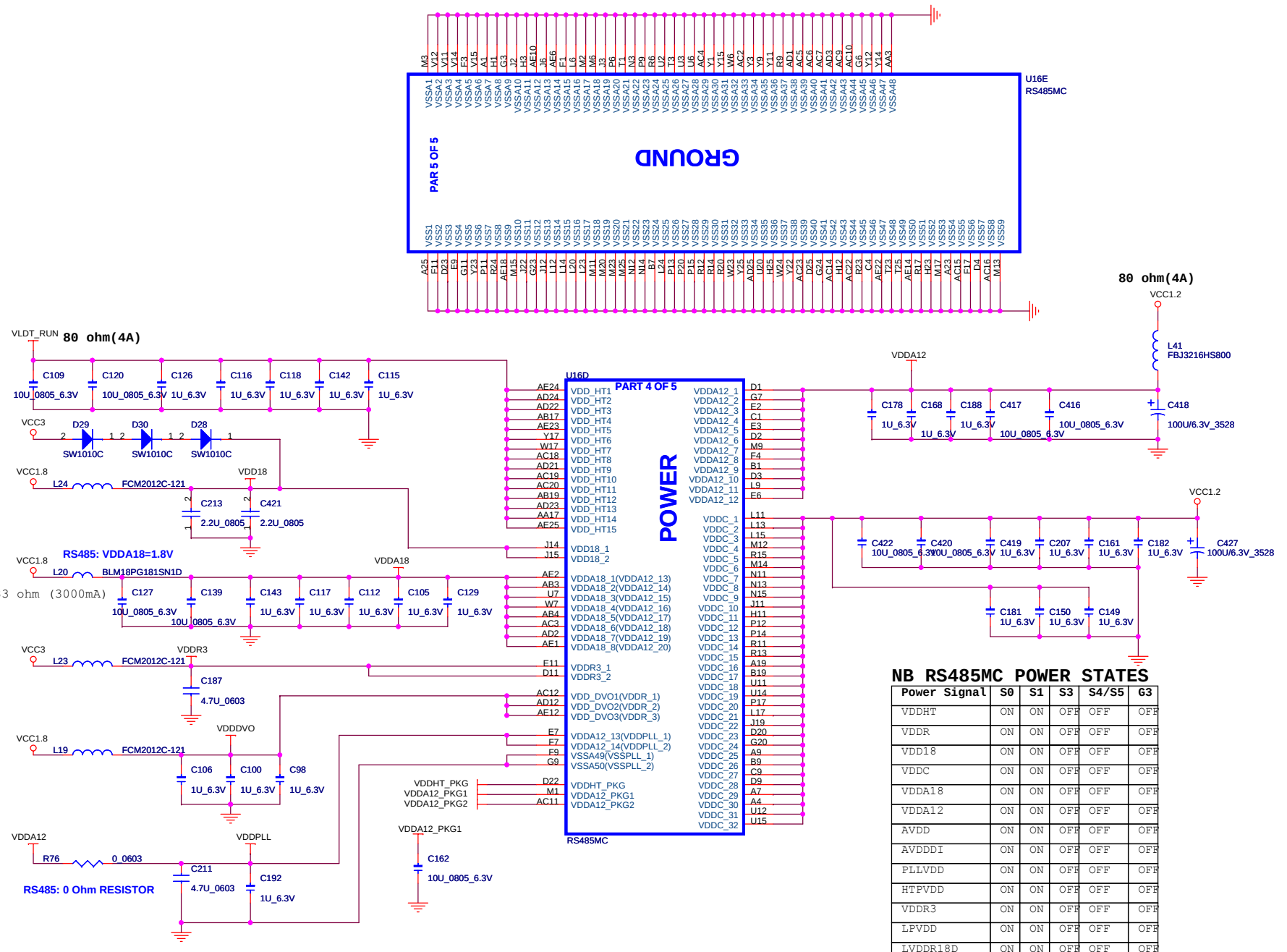
RS485MC only support two general purpose PCI-E links
GPP_TX[0:1]P GPP_RX[0:1]P
GPP_TX[0:1]N GPP_RX[0:1]N



Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: RS485MC PCIE LINK I/F	Rev: D
Date: Thursday, May 24, 2007	Sheet 11 of 35	



Quanta Computer Inc.			
PROJECT : ES2			
Size	Document Number		Rev
	RS485MC SYSTEM I/F & CLKGEN		D
Date: Thursday, May 24, 2007	Sheet 12	of 35	



NB RS485MC POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	RS485MC POWER	D
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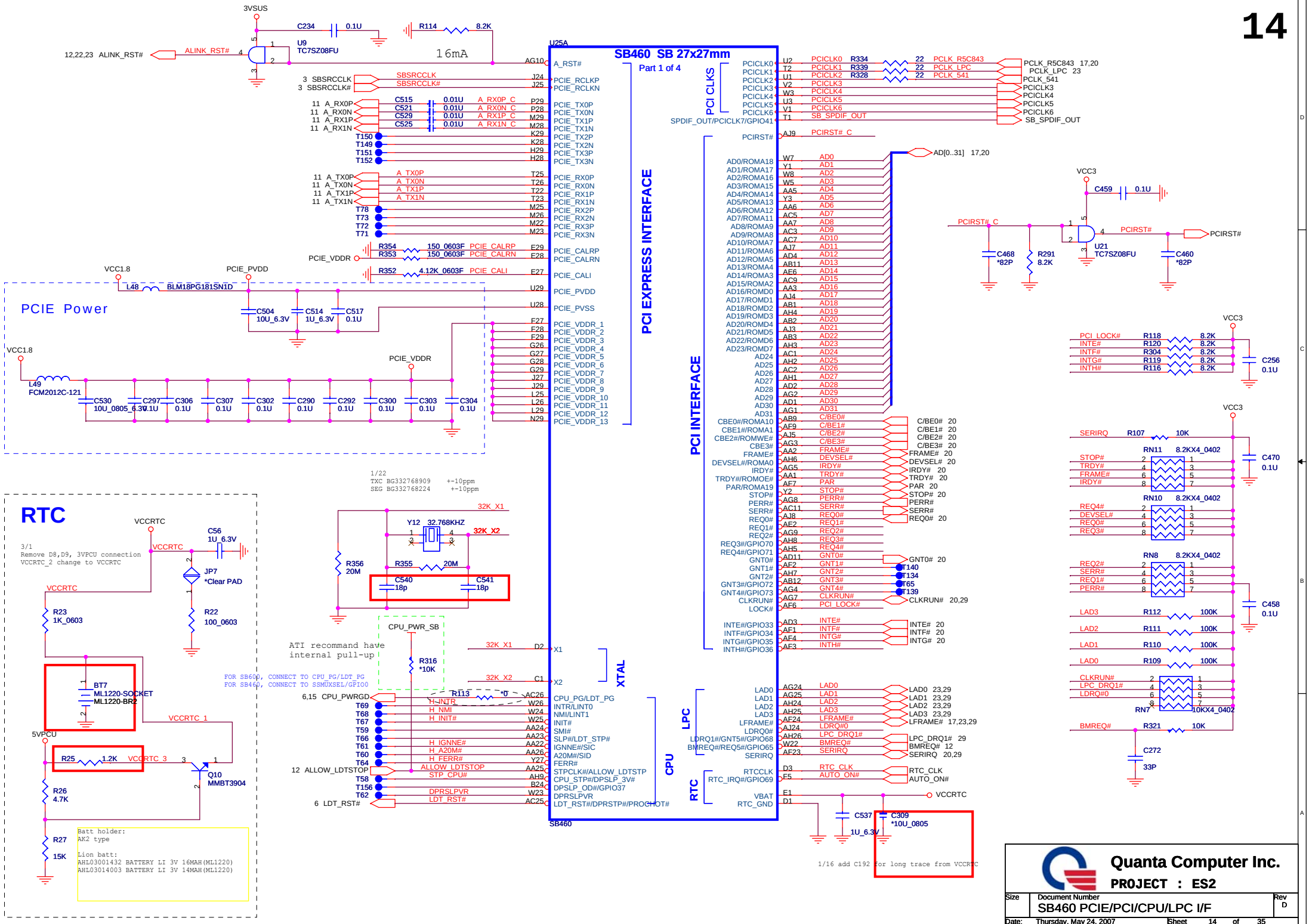
SB460 SB 27x27mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
SB460
PCIE Power
RTC
16mA
ATI recommand have internal pull-up
1/22
TXC BG332768909 +-10ppm
SEG BG332768224 +-10ppm
3/1
Remove D8,D9, 3VPCU connection
VCCRTC_2 change to VCCRTC
Batt holder:
AK2 type
Lion batt:
AHL03001432 BATTERY LI 3V 16MAH(ML1220)
AHL03014003 BATTERY LI 3V 14MAH(ML1220)
1/16 add C192 for long trace from VCCRTC
Quanta Computer Inc.
PROJECT : ES2
Document Number
SB460 PCIE/PCI/CPU/LPC I/F
Rev D
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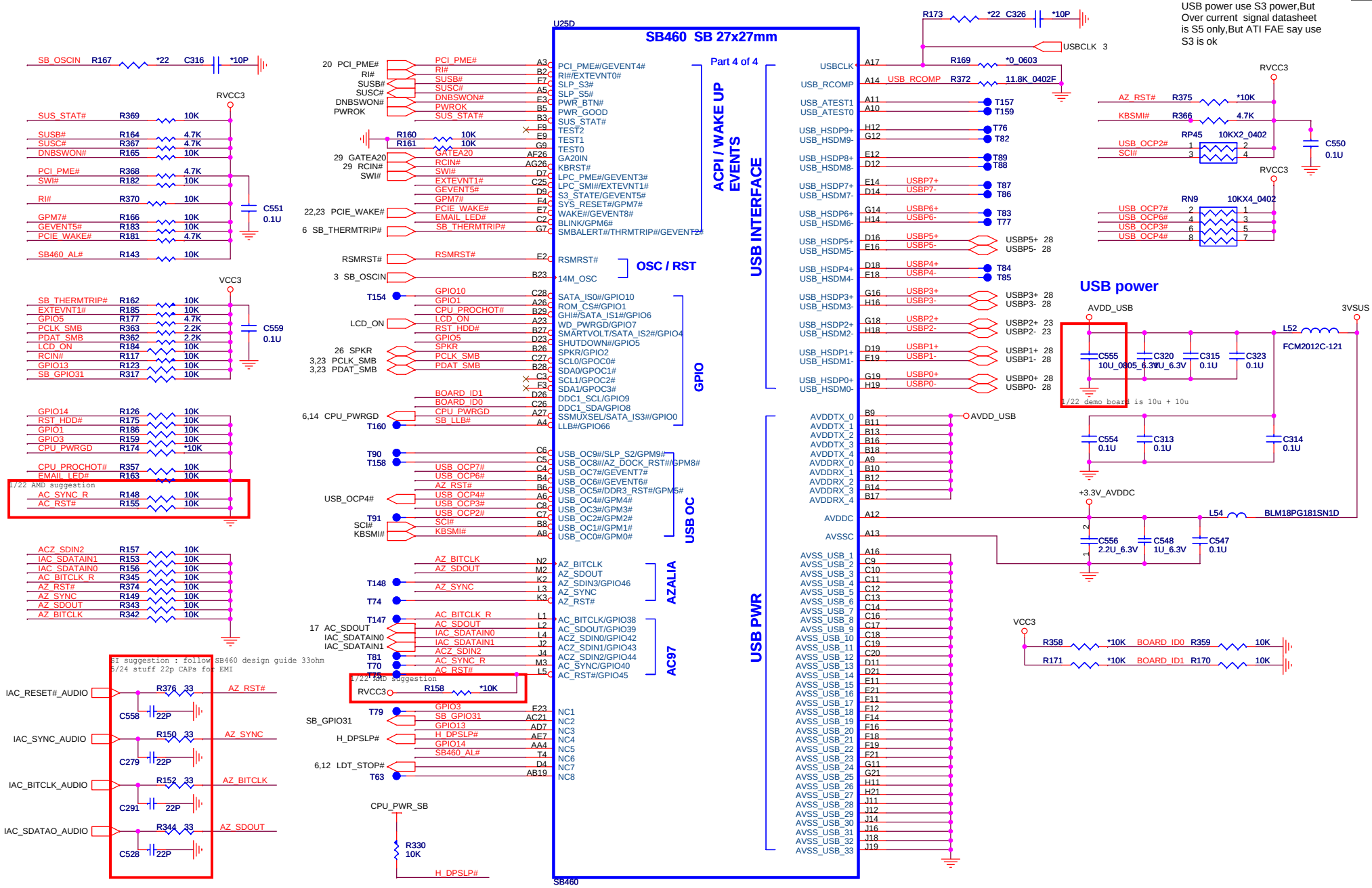
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok



Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: SB460 ACPI/GPIO/USB/AC97	Rev: D
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U25B

SB460 SB 27x27mm

Part 2 of 4

SERIAL ATA

ATA 66/100

SPI ROM

HW MONITOR

SERIAL ATA POWER

SATA_TXP0 SATA_TXN0 C237 C236 0.01U 0.01U SATA_TXP0_C SATA_TXN0_C AH21 AJ21

SATA_RXN0 SATA_RXP0 SATA_RXN0 SATA_RXP0 AH20 AJ20

T136 T126 AH18 AJ18

T133 T138 AH17 AJ17

T131 T130 AH13 AH14

T132 T137 AH16 AJ16

T127 T128 AJ11 AH11

T57 T135 AH12 AJ13

R122 1K/F SATA_CAL AF12

SATA_X1 AD16

SATA_X2 AD18

24,25 SATA_LED# AC12

PLLVDD_ATA AD14 AJ10

XTLVDD_ATA AC16

+1.8V_ATA AE14 AE16 AE18 AE19 AF19 AF21 AG22 AG23 AH22 AH23 AJ12 AJ14 AJ19 AJ22 AJ23

SATA_TX0+ SATA_TX0- SATA_RX0- SATA_RX0+ SATA_TX1+ SATA_TX1- SATA_RX1- SATA_RX1+ SATA_TX2+ SATA_TX2- SATA_RX2- SATA_RX2+ SATA_TX3+ SATA_TX3- SATA_RX3- SATA_RX3+ SATA_CAL SATA_X1 SATA_X2 SATA_ACT#/GPIO67

PLLVDD_SATA_1 PLLVDD_SATA_2 XTLVDD_SATA

AVDD_SATA_1 AVDD_SATA_2 AVDD_SATA_3 AVDD_SATA_4 AVDD_SATA_5 AVDD_SATA_6 AVDD_SATA_7 AVDD_SATA_8 AVDD_SATA_9 AVDD_SATA_10 AVDD_SATA_11 AVDD_SATA_12 AVDD_SATA_13 AVDD_SATA_14 AVDD_SATA_15

AVSS_SATA_1 AVSS_SATA_2 AVSS_SATA_3 AVSS_SATA_4 AVSS_SATA_5 AVSS_SATA_6 AVSS_SATA_7 AVSS_SATA_8 AVSS_SATA_9 AVSS_SATA_10 AVSS_SATA_11 AVSS_SATA_12 AVSS_SATA_13 AVSS_SATA_14 AVSS_SATA_15 AVSS_SATA_16 AVSS_SATA_17 AVSS_SATA_18 AVSS_SATA_19 AVSS_SATA_20 AVSS_SATA_21 AVSS_SATA_22 AVSS_SATA_23 AVSS_SATA_24 AVSS_SATA_25 AVSS_SATA_26 AVSS_SATA_27

IDE_IORDY IDE_IRQ IDE_A0 IDE_A1 IDE_A2 IDE_DACK# IDE_DRQ IDE_IOR# IDE_IOW# IDE_CS1# IDE_CS3#

AB29 PIORDY AA28 IRQ14 AA29 PDA0 AB27 PDA1 Y28 PDA2 AB28 PDDACK# AC27 PDDREQ AC29 PDIOR# AC28 PDIOW# W28 PDCS1# W27 PDCS3#

PIORDY IRQ14 PDA0 25 PDA1 25 PDA2 25 PDDACK# 17,25 PDDREQ 25 PDIOR# 25 PDIOW# 25 PDCS1# 25 PDCS3# 25 PDD[0..15] 25

IDE_D0/GPIO15 IDE_D1/GPIO16 IDE_D2/GPIO17 IDE_D3/GPIO18 IDE_D4/GPIO19 IDE_D5/GPIO20 IDE_D6/GPIO21 IDE_D7/GPIO22 IDE_D8/GPIO23 IDE_D9/GPIO24 IDE_D10/GPIO25 IDE_D11/GPIO26 IDE_D12/GPIO27 IDE_D13/GPIO28 IDE_D14/GPIO29 IDE_D15/GPIO30

AD28 PDD0 AD26 PDD1 AE29 PDD2 AE27 PDD3 AG29 PDD4 AH28 PDD5 AJ28 PDD6 AJ27 PDD7 AH27 PDD8 AG27 PDD9 AG28 PDD10 AF28 PDD11 AF29 PDD12 AE28 PDD13 AD25 PDD14 AD29 PDD15

SPI_DI/GPIO12 SPI_DO/GPIO11 SPI_CLK/GPIO47 SPI_HOLD#/GPIO31 SPI_CS#/GPIO32

J3 J6 G3 G2 G6

LAN_RST#/GPIO13 ROM_RST#/GPIO14

C23 G5

FANOUT0/GPIO3 FANOUT1/GPIO48 FANOUT2/GPIO49

M4 T3 V4

FANIN0/GPIO50 FANIN1/GPIO51 FANIN2/GPIO52

N3 P2 W4

TEMP_COMM TEMPIN0/GPIO61 TEMPIN1/GPIO62 TEMPIN2/GPIO63 TEMPIN3/TALERT#/GPIO64

P5 P7 P8 T8 T7

VIN0/GPIO53 VIN1/GPIO54 VIN2/GPIO55 VIN3/GPIO56 VIN4/GPIO57 VIN5/GPIO58 VIN6/GPIO59 VIN7/GPIO60

V5 L7 M8 V6 M6 P4 M7 V7

AVDD N1

AVSS M1

SB460

SB-3

SATA Power

VCC1.8 L43 BLM18PG181SN1D XTLVDD_ATA C469 10U_0805_6.3V C268 1U_6.3V

VCC1.8 L44 BLM18PG181SN1D PLLVDD_ATA C462 10U_0805_6.3V C267 1U_6.3V

VCC1.8 L32 FCM2012C-121 +1.8V_ATA C238 10U_0805_6.3V C243 0.1U C241 0.1U C252 0.1U C249 0.1U C242 0.1U C248 0.1U

SATA clock Option

12/5 modify
Remove OSC. option to save layout space

C464 22P C463 22P Y9 25MHZ R289 10M SATA_X1 SATA_X2

L45 FBJ3216HS800 80ohm/4A VCC3 C472 100U/6.3V_3528 VDDQ_3V

C287 C275 C270 C296 C240 0.1U

C281 C277 C263 C271 C269 C317 0.1U

C321 C251 C266 C250 C308 C244 0.1U

D27 PJMBZ5V6(SOT-23)

L46 FBJ3216HS800 80ohm/4A VCC1.8 C488 100U/6.3V_3528 VDD_1.8V

C485 10U_0805_6.3V C276 C294 C289 C293 1U_6.3V

C280 C283 C278 C274 C282 C285 0.1U

C284 C273 0.1U

RVCC3 L53 BLM18PG181SN1D SB_S5_3V C544 10U_0805_6.3V C305 C319 C298 C301 C299 0.1U

RVCC1.8 L50 BLM18PG181SN1D SB_S5_1.8V C538 10U_6.3V C536 C539 C534 0.1U

1.8VUSB_PHY

VCC1.2 R337 0 CPU_PWR_SB C498 0.1U CPU_PWR V5_VREF AVDDCK_3.3V AVDDCK_1.2V AVSSCK

AVDD_CK_1.8V VCC1.8 L51 BLM18PG181SN1D C543 2.2U_6.3V C324 1U_6.3V C325 0.1U

U25C

SB4600 SB 27x27mm

Part 3 of 4

POWER

A25 A28 C29 D24 L9 L21 M5 P3 P9 T5 V9 W2 W6 W21 W29 AA12 AA16 AA19 AC4 AC23 AD27 AE1 AE9 AE23 AH29 AJ2 AJ6 AJ26 VDDQ_2 VDDQ_3 VDDQ_4 VDDQ_5 VDDQ_6 VDDQ_7 VDDQ_8 VDDQ_9 VDDQ_10 VDDQ_11 VDDQ_12 VDDQ_13 VDDQ_14 VDDQ_15 VDDQ_16 VDDQ_17 VDDQ_18 VDDQ_19 VDDQ_20 VDDQ_21 VDDQ_22 VDDQ_23 VDDQ_24 VDDQ_25 VDDQ_26 VDDQ_27 VDDQ_28

M13 M17 N12 N15 N18 R13 R17 U12 U15 U18 V13 V17 VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

A2 A7 F1 J5 J7 K1 S5_3.3V_1 S5_3.3V_2 S5_3.3V_3 S5_3.3V_4 S5_3.3V_5 S5_3.3V_6

G4 H1 H2 H3 S5_1.2V_1 S5_1.2V_2 S5_1.2V_3 S5_1.2V_4

A18 A19 B19 B20 B21 USB_PHY_1.2V_1 USB_PHY_1.2V_2 USB_PHY_1.2V_3 USB_PHY_1.2V_4 USB_PHY_1.2V_5

AA27 AE11 A24 A22 B22

V29 V28 V27 V26 V25 V24 V23 V22 U27 T29 T28 T27 T24 T21 P27 PCIE_VSS_42 PCIE_VSS_41 PCIE_VSS_40 PCIE_VSS_39 PCIE_VSS_38 PCIE_VSS_37 PCIE_VSS_36 PCIE_VSS_35 PCIE_VSS_34 PCIE_VSS_33 PCIE_VSS_32 PCIE_VSS_31 PCIE_VSS_30 PCIE_VSS_29 PCIE_VSS_28

A1 A20 A21 A29 B1 B7 B25 C21 C22 C24 D6 E24 F2 F23 G1 J1 J8 L6 L8 M9 M12 M15 M18 N13 N17 P1 P6 P21 R12 R15 R18 T6 T9 U13 U17 V3 V8 V12 V15 V18 V21 W1 W9 Y29 AA11 AA14 AA18 AC6 AC24 AD9 AD23 AE3 AE27 AG6 AJ1 AJ25 AJ29

D27 D28 D29 F26 G23 G24 G25 H27 J23 J26 J28 K27 L22 L23 L24 L27 L28 M21 M24 M27 N27 N28 P22 P23 P24 P25 P26 PCIE_VSS_1 PCIE_VSS_2 PCIE_VSS_3 PCIE_VSS_4 PCIE_VSS_5 PCIE_VSS_6 PCIE_VSS_7 PCIE_VSS_8 PCIE_VSS_9 PCIE_VSS_10 PCIE_VSS_11 PCIE_VSS_12 PCIE_VSS_13 PCIE_VSS_14 PCIE_VSS_15 PCIE_VSS_16 PCIE_VSS_17 PCIE_VSS_18 PCIE_VSS_19 PCIE_VSS_20 PCIE_VSS_21 PCIE_VSS_22 PCIE_VSS_23 PCIE_VSS_24 PCIE_VSS_25 PCIE_VSS_26 PCIE_VSS_27

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57

SB460

V5_VREF

VCC5 R290 1K/F V5_VREF

VCC3 D35 SW1010C C239 1U_6.3V C254 0.1U

1.8VUSB_PHY

1.8VSUS L35 BLM18PG181SN1D D47 *ESD SOD523 C327 10U_0805_6.3V

1.8VUSB_PHY C318 0.1U C312 0.1U C310 0.1U

Quanta Computer Inc.

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	SB460 HDD/POWER/DECOUPLING	D

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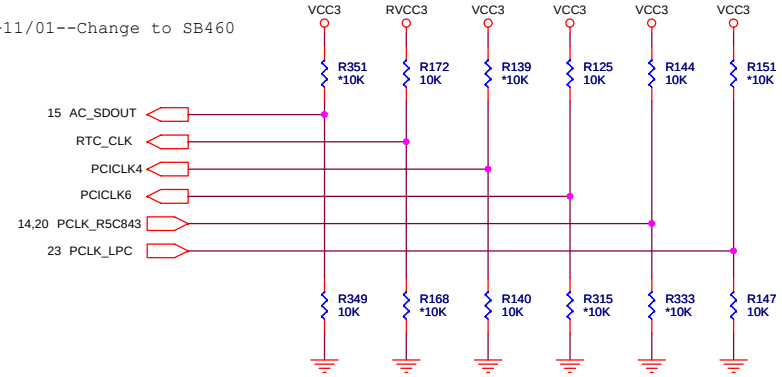
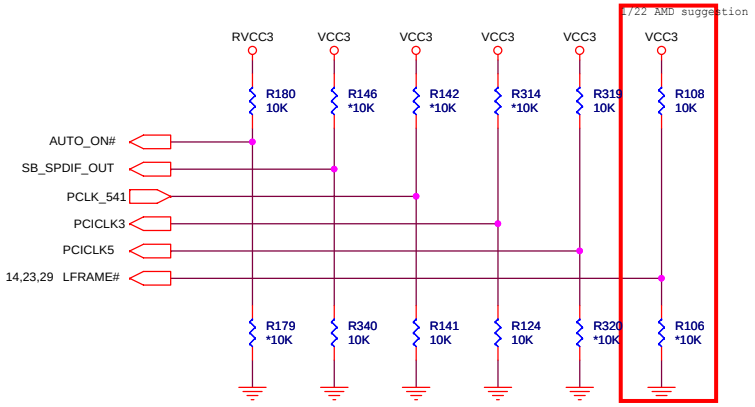
Edison-11/01--Change to SB460

REQUIRED STRAPS



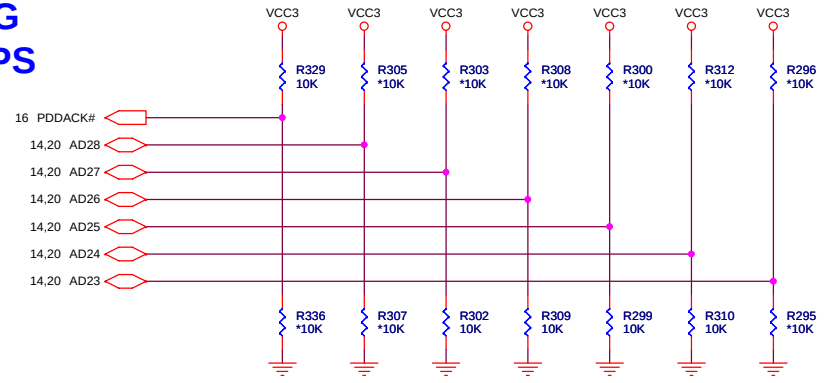
	AC_SDOUT	RTC_CLK	PCICLK4	PCICLK6	PCLK_R5C843 PCLK_LPC PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	



	AUTO_ON#	SB_SPDIF_OUT	PCLK_541	PCICLK3	PCICLK5	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP

DEBUG STRAPS



	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

SB-4

Quanta Computer Inc.
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	SB460 STRAPS	D
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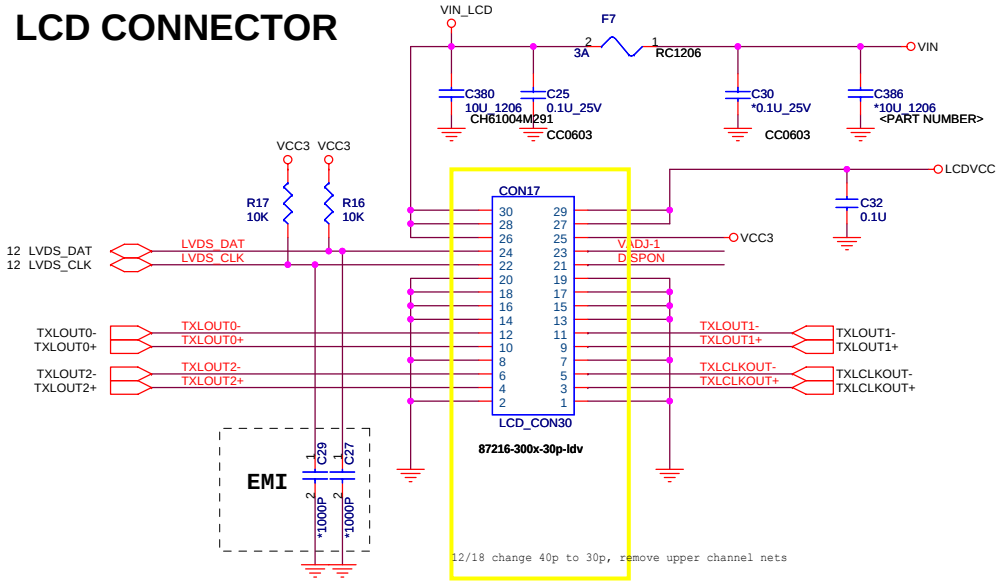
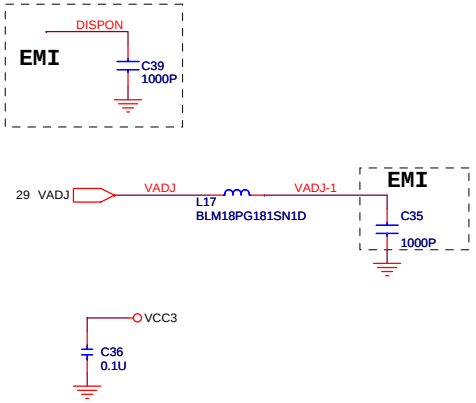
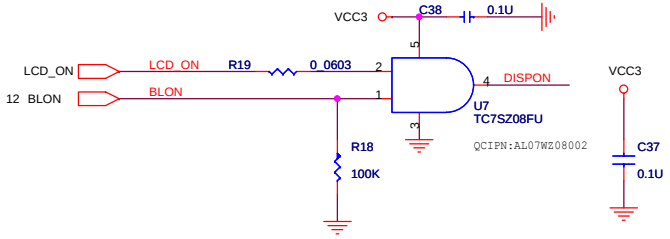
LCD CONNECTOR

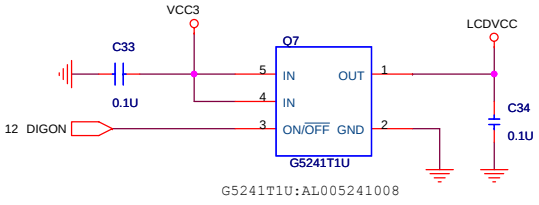




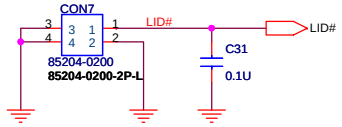
BACKLIGHT CONTROL



PANEL VCC CONTROL



LID



Quanta Computer Inc.
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Size	Document Number	Rev
	LCD PANEL	D
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CRT

12/8 modify
CX00070B0008 MLB-160808-0070B-N3 OBS
CX08B75000I TB160808B750 (75 0hm BQ2A)
CX808600101 KCE#FBM-10-160808-600T(60 ohm) - current use (PL1)

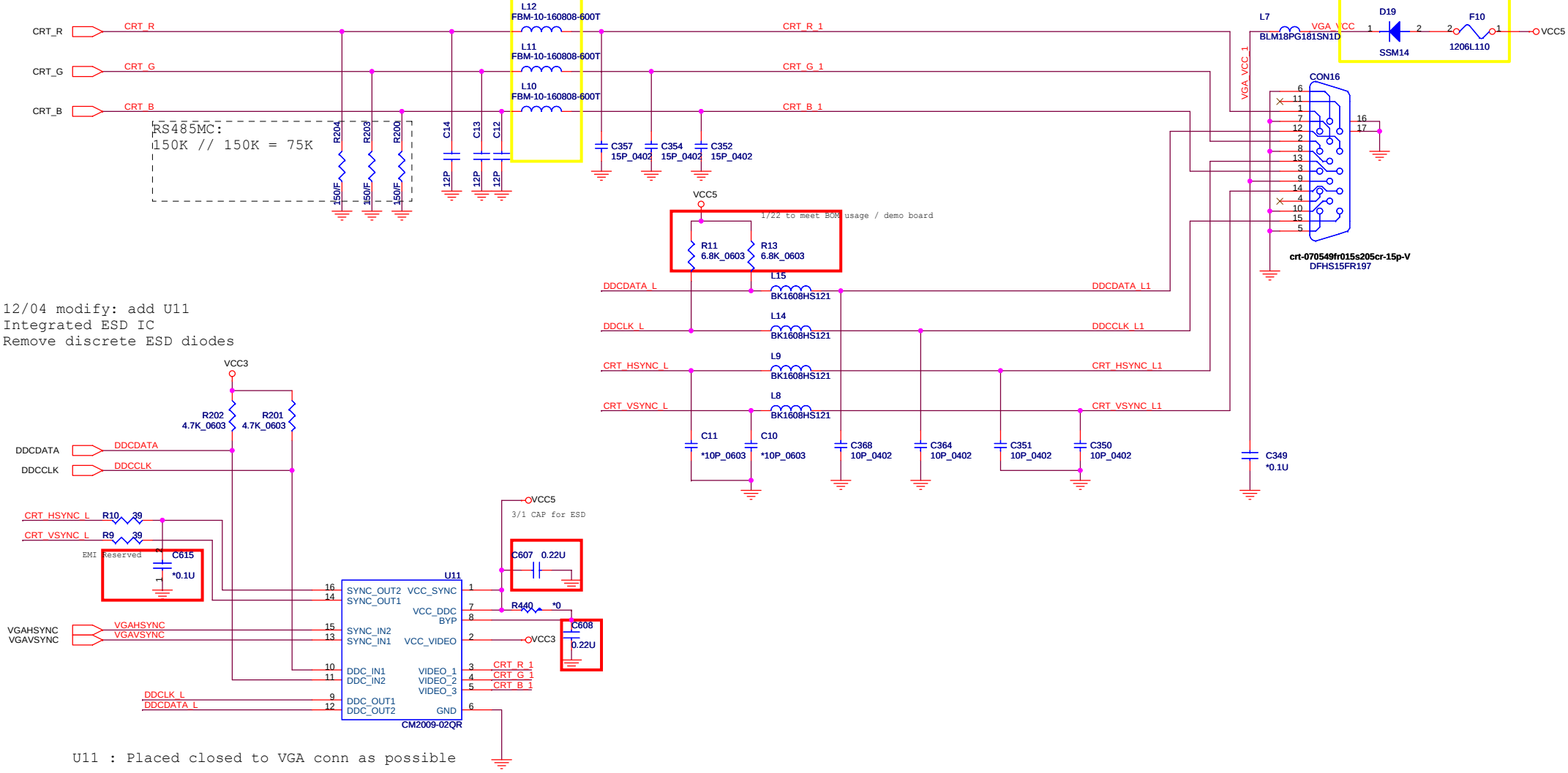
12/5 modify F10
DK110TPU110 - SMD1812P110TF(KW3S) to
DKZ00TFU101(littlefuse)
1812 to 1206

D19
KW3SBC1SS355Z051SS355(80V,100MA) to
PL1BC0SSM14Z30SSM14PT(40V,1A)

RS485MC:
150K // 150K = 75K

12/04 modify: add U11
Integrated ESD IC
Remove discrete ESD diodes

U11 : Placed closed to VGA conn as possible



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	CRT	D
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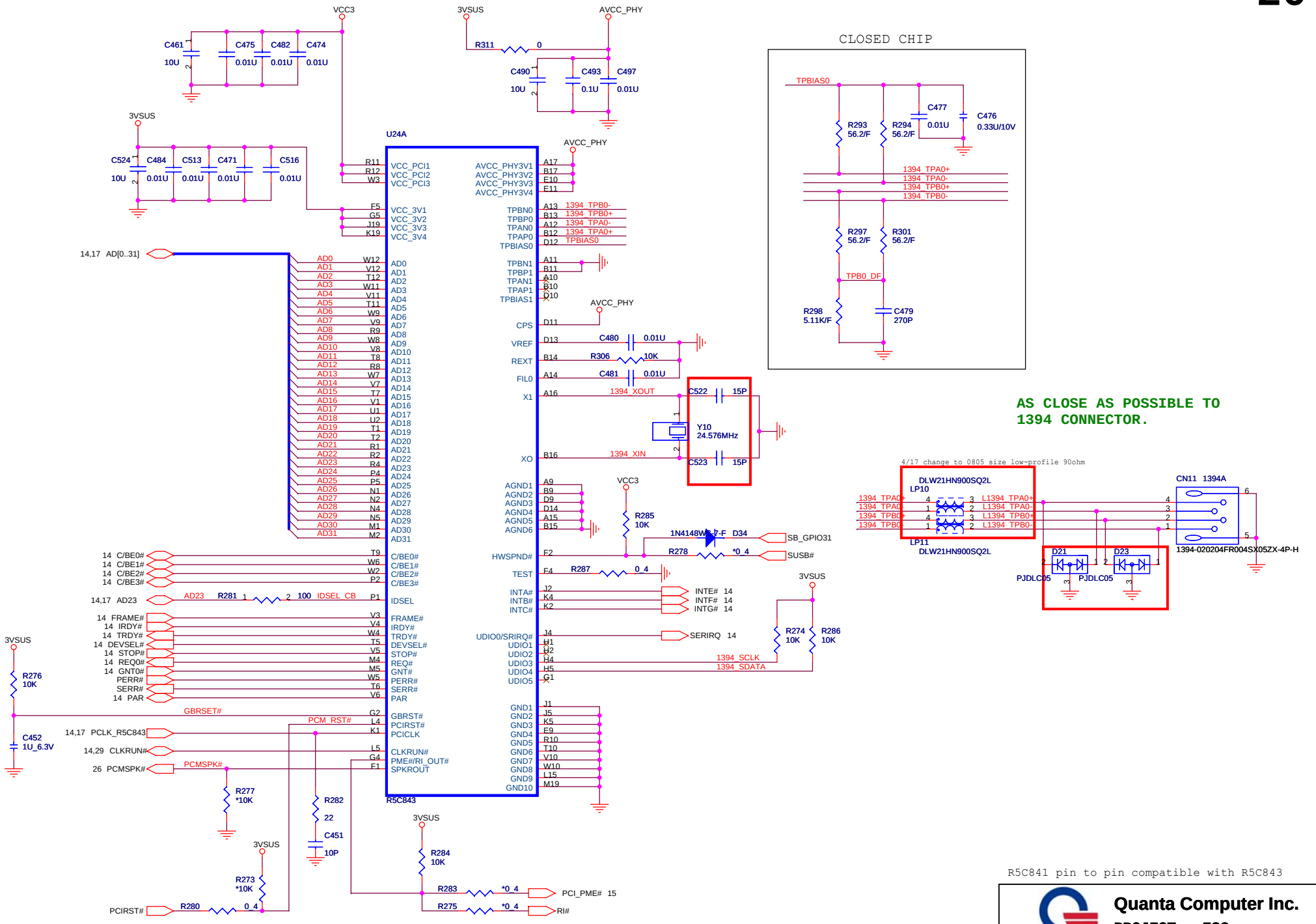

CLOSED CHIP

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

R5C841 pin to pin compatible with R5C843

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: R5C843 PCI/1394	Rev: D
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PCMCIA Conn.

01/02 change Footprint to AK2 CardBus symbol, DFHS68FR563 PC Card Frame

CN7
PCI-1CA4A5AG1-WR-4F-84P

U24B
R5C843

Shield GND

R338 47

A_VCC

C494 0.01U
C491 *10U

A_VPP

C508 0.01U

C546 270pF
C457 270pF
C531 0.01U

Place near the Slot A VCC pins

C492 10U
C495 *1000P_4
C520 0.1U
C519 0.1U

Place near the Slot A VPP pins

C509 10U
C506 *1000P_4
C507 0.1U

1/10 This is for MS-PRO short issue

Q20
NC7WB66K8X_NL

U23
G5240B1T1U
AL005240010

C486 0.1U
C473 0.1U
C478 10U/10V

MS Socket

CON22A

R235 10K
R239 33

SD Socket

CON22B

R253 470K
R237 10K

4/17
33ohm to 56 ohm
22p stuff for EMI SD issue

R335 56
R437 56
R441 56
R313 56
R318 56
R265 10K
R341 150K

C503 22P
C624 22P
C625 22P
C626 22P
C627 22P

EC37
Q19
ME2N7002E

	MDIO00	MDIO01
SD/MMC	L	H
MS	H	L
xD	L	L

XD Socket

4IN1-R012-210-XX-44P

CON22C

R238 33K

Q18
ME2N7002E

D31
1N4148WS-7-F

1N4148WS-7-D32
1N4148WS-7-D33

Not-Support 12V

U26
R5531V002

Place near the Power IC R5531V pins

R348 100K
R288 0
R272 10K

U24C
R5C843

Quanta Computer Inc.
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	R5C843 PCMCIA/4 IN 1	D

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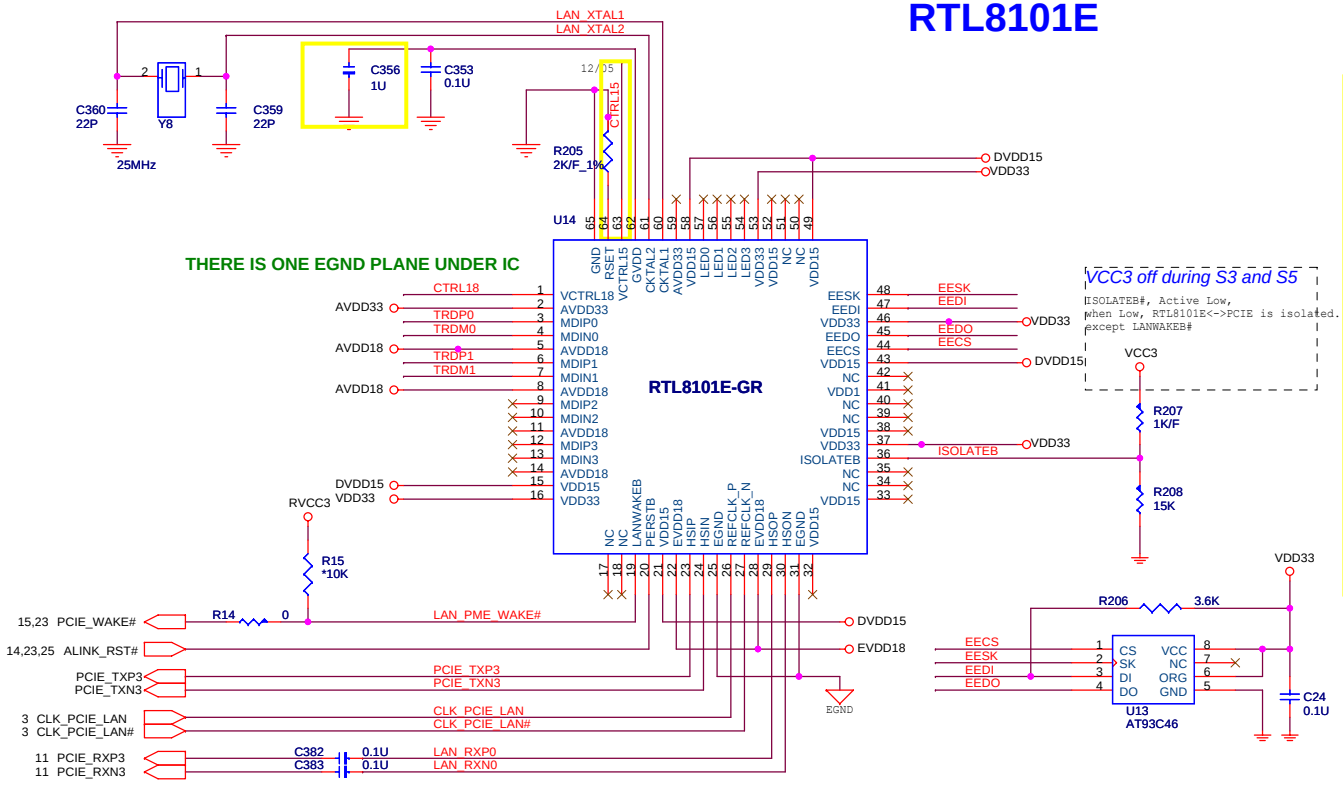
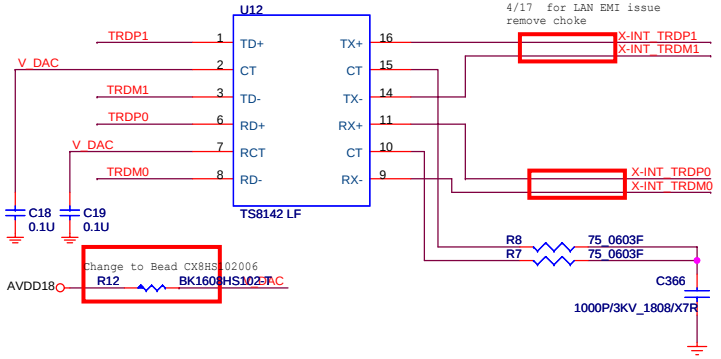
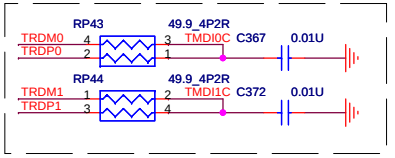
RTL8101E



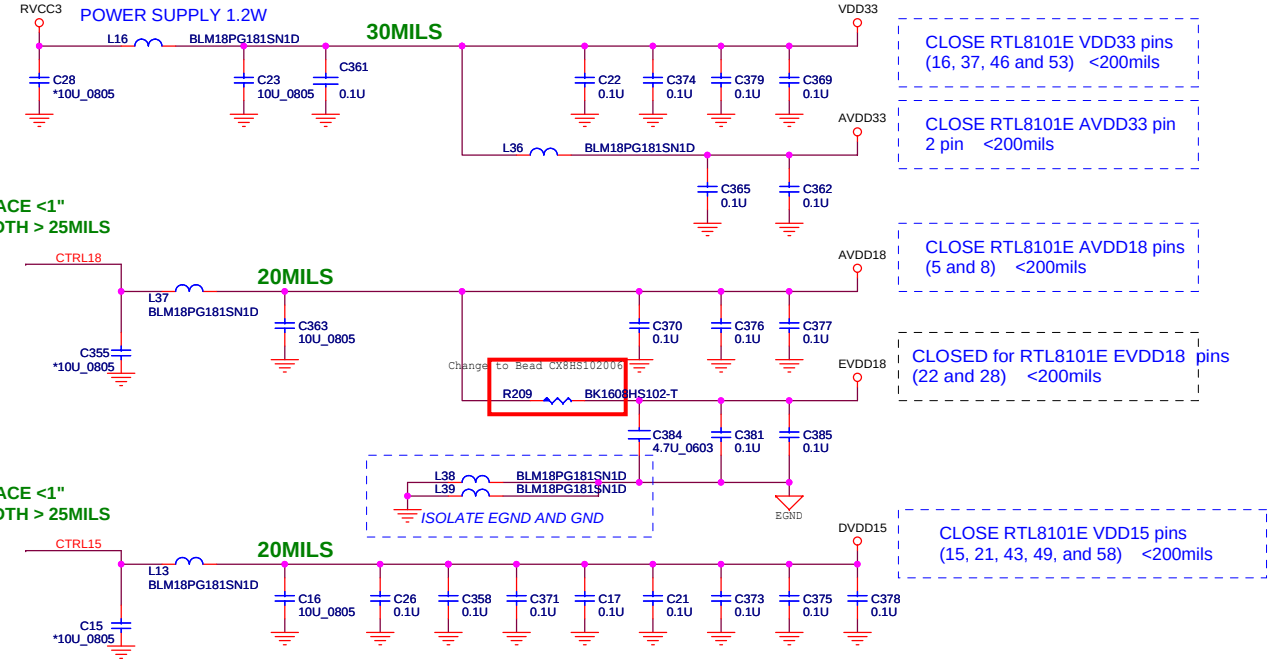
6 coil transformer:
BOT TS8142 LF (DB0YV1LAN01)
BYT 11F-0606(DB0ES2LAN02)



These parts only for RTL8101E application



POWER SUPPLY



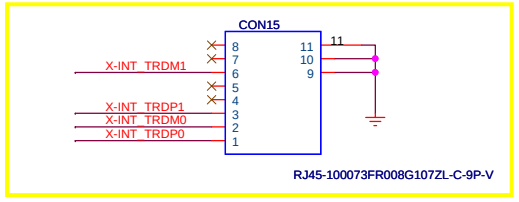
CLOSE RTL8101E VDD33 pins
(16, 37, 46 and 53) <200mils

CLOSE RTL8101E AVDD33 pin
2 pin <200mils

CLOSE RTL8101E AVDD18 pins
(5 and 8) <200mils

CLOSED for RTL8101E EVDD18 pins
(22 and 28) <200mils

CLOSE RTL8101E VDD15 pins
(15, 21, 43, 49, and 58) <200mils



RTL8101E P/N:AL08101E005

RTL8101E is 10/100 Base, RTL8111B is Giga Base
RTL8101E and RTL8111B are pin to pin compatible

Quanta Computer Inc.
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	LAN RTL8101E	D
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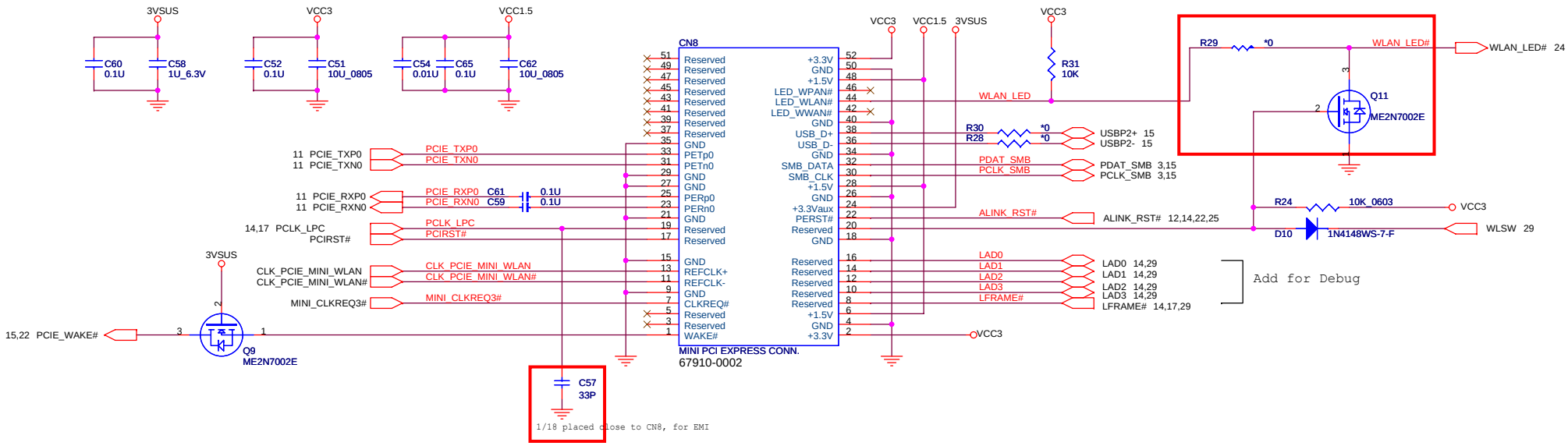
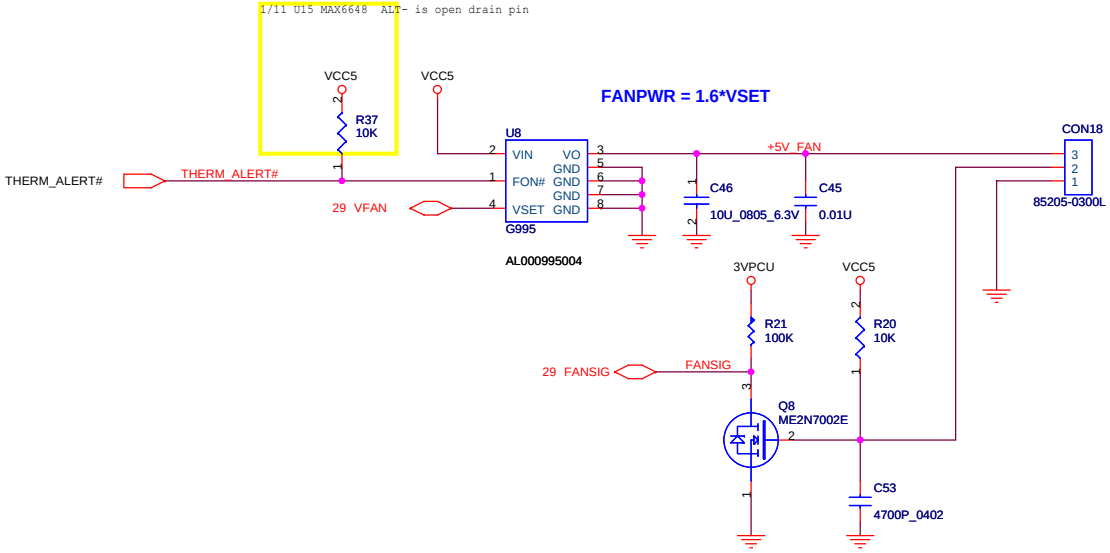
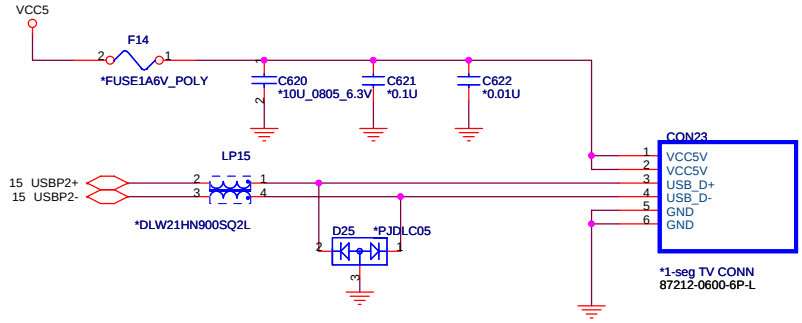
Mini PCI-E Card WLAN



FAN CONN

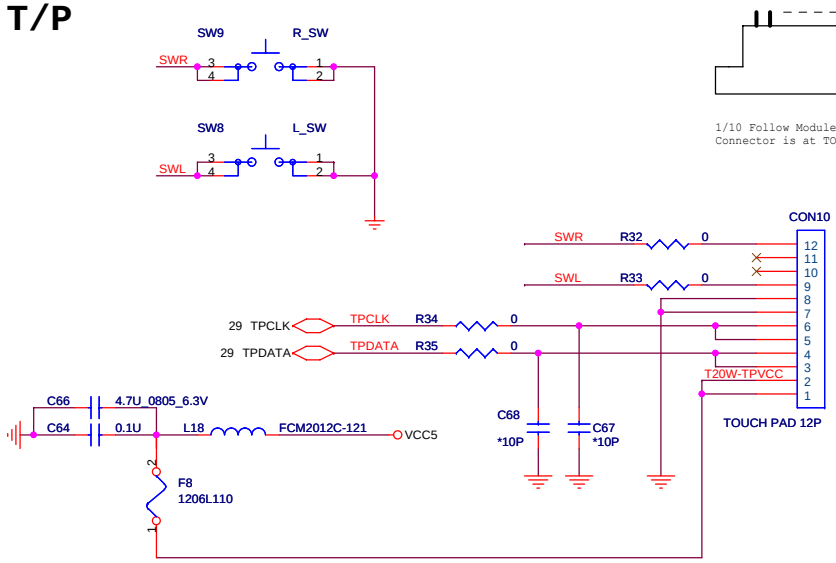


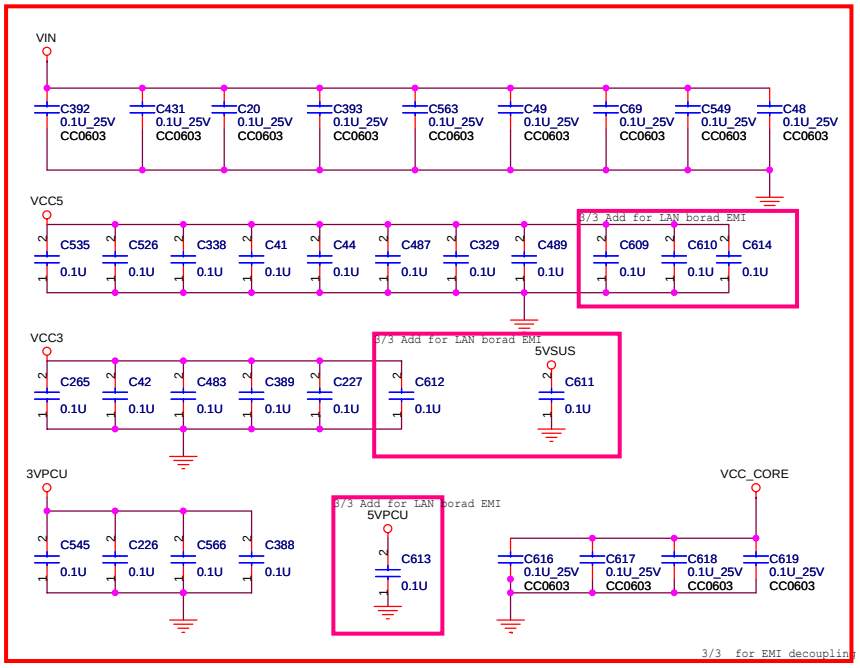
One segment TV (Pixela)



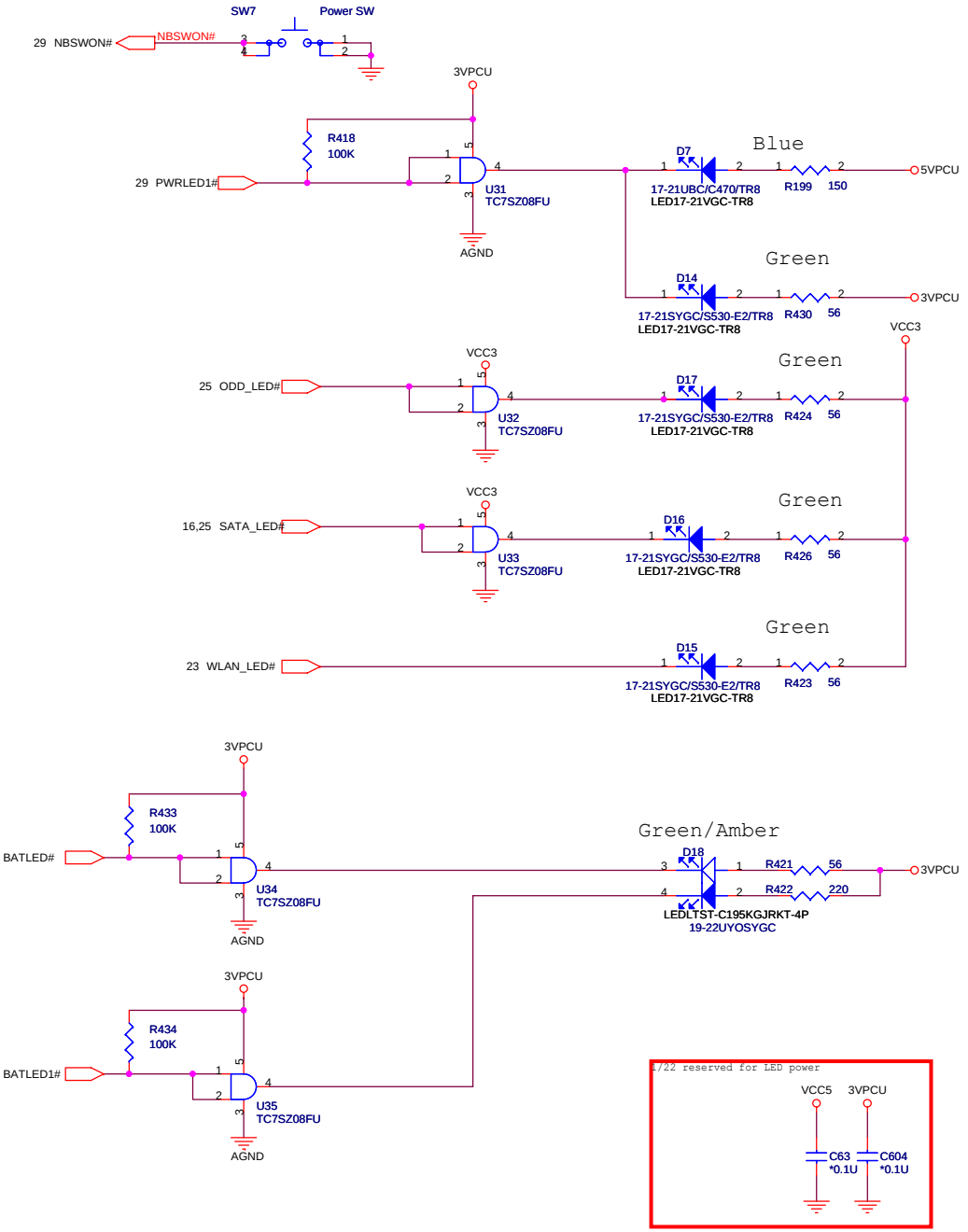
Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: FAN / MINI PCIE / 1-seg TV	Rev D
Date: Thursday, May 24, 2007	Sheet 23 of 35	

T/P





SYSTEM LEDs



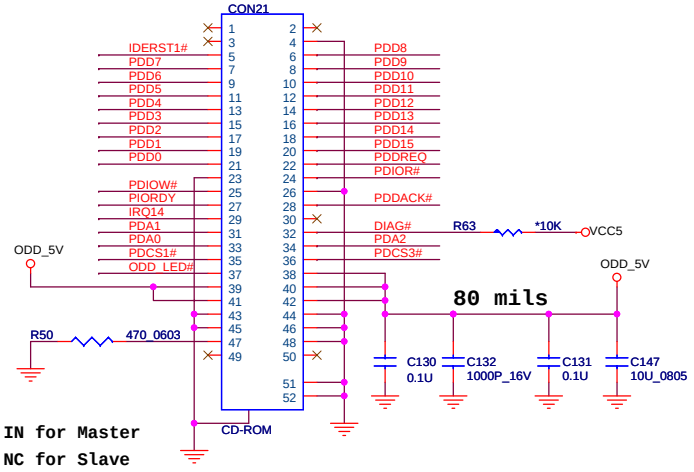
POWER LED	BATT LED	Wireless LED	HDD LED	ODD LED	POWER SWITCH
D14	D18	D15	D16	D17	D7

Quanta Computer Inc.
PROJECT : ES2

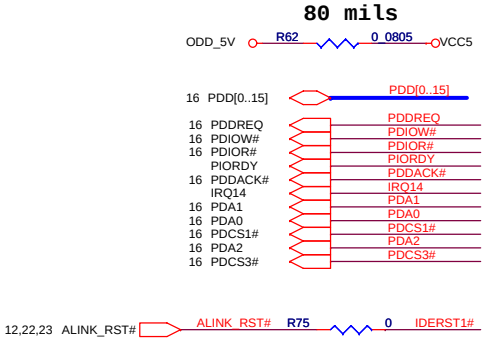
Size	Document Number	Rev
	LEDs / TP CONNECTOR	A
Date: Thursday, May 24, 2007	Sheet 24 of 35	

CD-ROM CONNECTOR

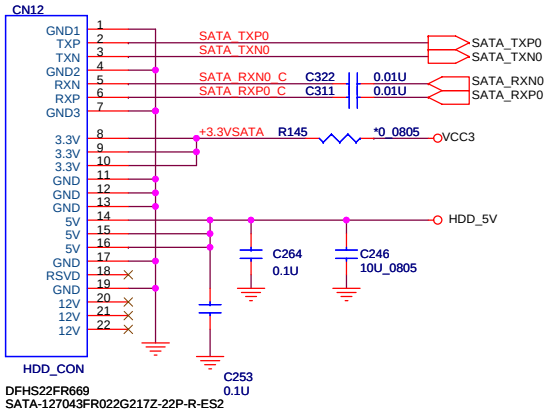
SMT TYPE CNN

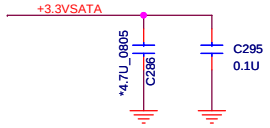


80 mils

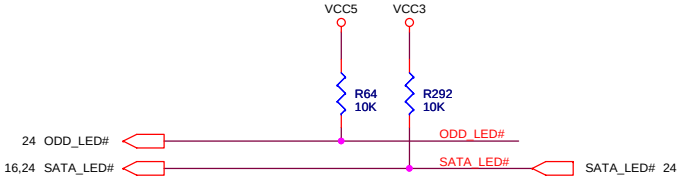


SATA HDD





40 mils



Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	ODD/SATA HDD	D
Date: Thursday, May 24, 2007	Sheet 25 of 35	

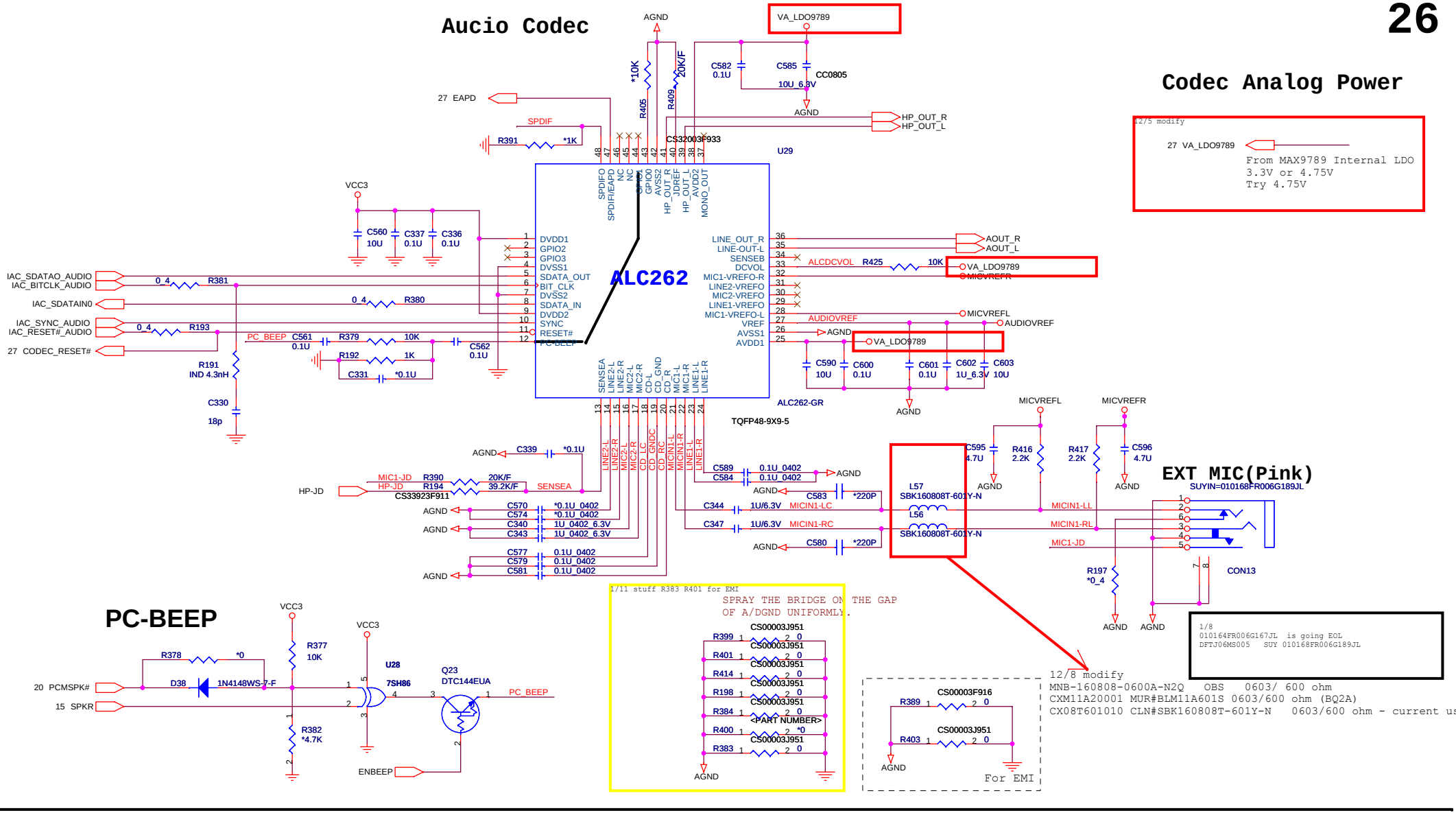
Aucio Codec

Codec Analog Power

12/5 modify

27 VA_LDO9789

From MAX9789 Internal LDO
3.3V or 4.75V
Try 4.75V



1/8
010164FR006G167JL is going EOL
DFTJ06MS005 SUY 010168FR006G189JL

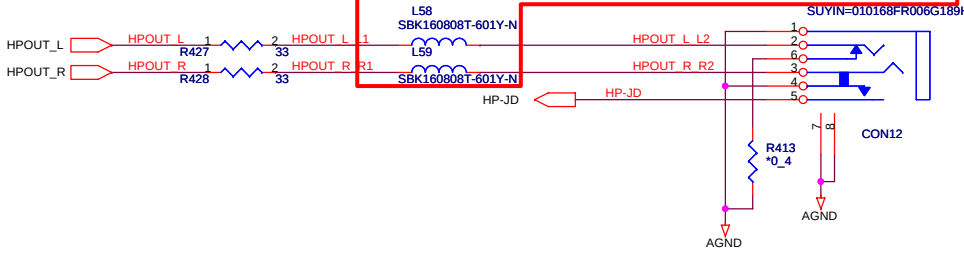
1/11 stuff R383 R401 for EMI

SPRAY THE BRIDGE ON THE GAP
OF A/DGND UNIFORMLY.

12/8 modify
MNB-160808-0600A-N2Q OBS 0603/ 600 ohm
CXM11A20001 MUR#BLM11A601S 0603/600 ohm (BQ2A)
CX08T601010 CLN#SBK160808T-601Y-N 0603/600 ohm - current use

PC-BEEP

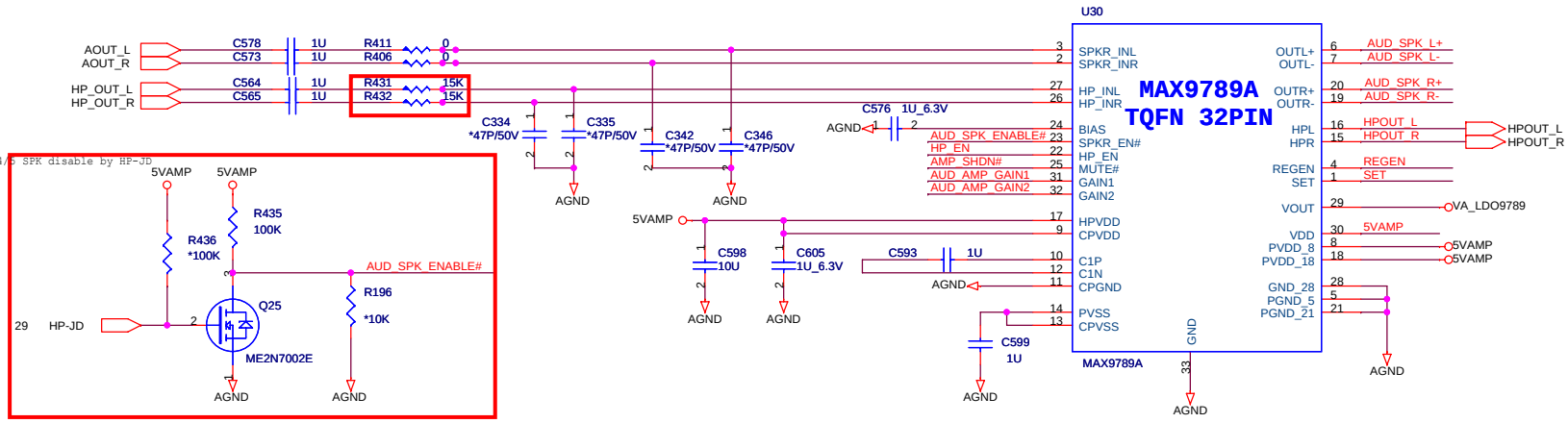
12/8 modify
MNB-160808-0600A-N2Q OBS 0603/ 600 ohm
CXM11A20001 MUR#BLM11A601S 0603/600 ohm (BQ2A)
CX08T601010 CLN#SBK160808T-601Y-N 0603/600 ohm - current use



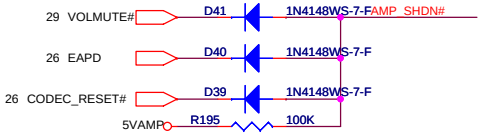
1/8
010164FR006G167HL is going EOL
DFTJ06MS004 SUY 010168FR006G189HL

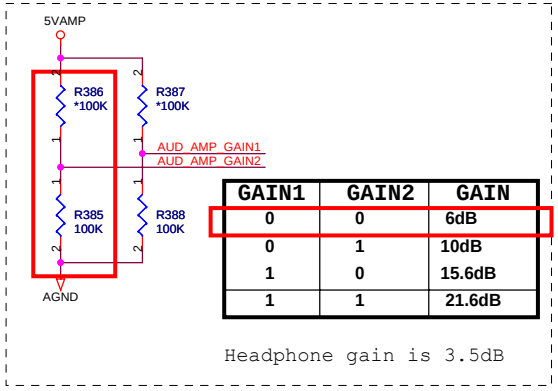
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	AUDIO ALC262 MIC/HP	D
Date: Thursday, May 24, 2007	Sheet 26 of 35	



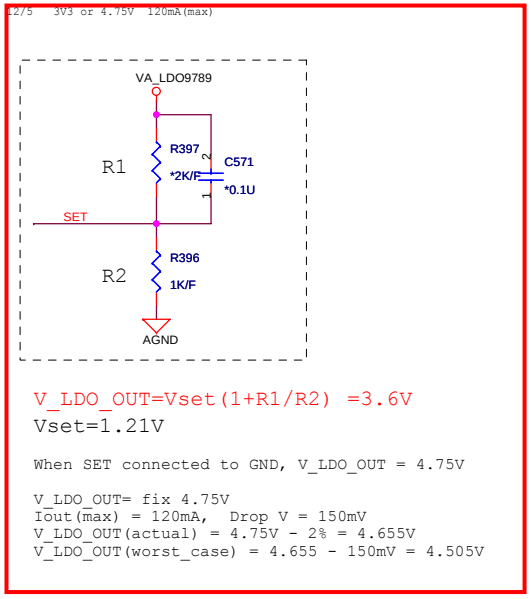
Head phone AMP always ON





GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

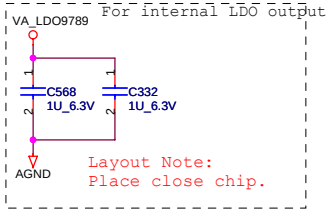
Headphone gain is 3.5dB

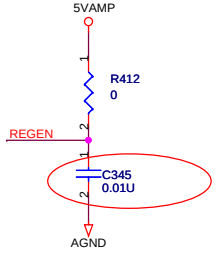


V_LDO_OUT=Vset(1+R1/R2) =3.6V
Vset=1.21V

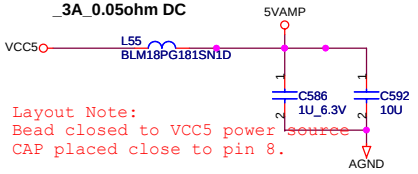
When SET connected to GND, V_LDO_OUT = 4.75V

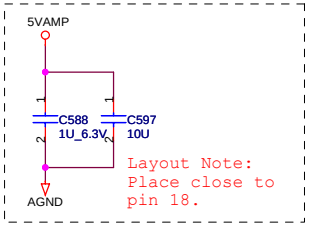
V_LDO_OUT= fix 4.75V
Iout(max) = 120mA, Drop V = 150mV
V_LDO_OUT(actual) = 4.75V - 2% = 4.655V
V_LDO_OUT(worst_case) = 4.655 - 150mV = 4.505V

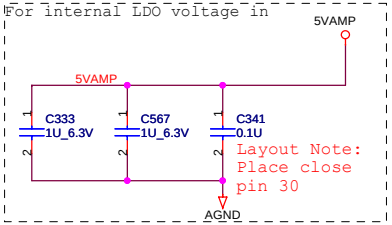


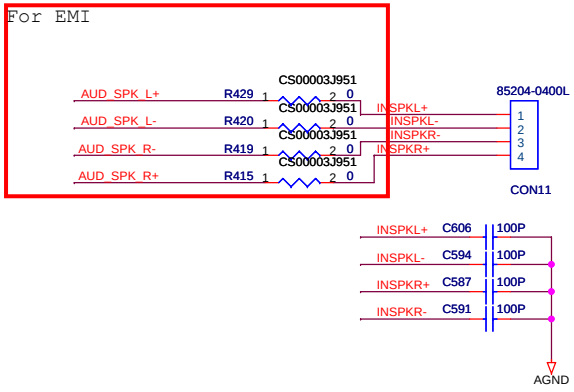


Enable Internal LDO









Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	AUDIO AMP/SPEAKER	D

Date: Thursday, May 24, 2007 Sheet 27 of 35

12/27 USBVCC3,5 and USBVCC5,7 swapped to use different CAP

3/4 swap pin net to correct footprint

5VSUS — F11 1206L110 — USBVCC5 — 40 mils

5VSUS — F12 1206L110 — USBVCC7 — 40 mils

5VSUS — 80 mils — F9 1206L110 — USBVCC1 — 40 mils

F13 1206L110 — USBVCC3 — 40 mils

C415 0.1U, C119 0.1U, C413 150U/6.3V CH71511MJ86

USBVCC5 — 150u to 100u — C9 0.1U, C348 100U/6.3V_3528

USBVCC7 — 150u to 100u — C47 0.1U, C387 100U/6.3V_3528

D24 PJDLC05 — LP8 DLW21HN900SQ2L — 15 USBP0+ / 15 USBP0- — USBVCC1 — C403 *47P, C408 *47P — CON19 USB usb-020173mr004s582zl-c2-4p-l-h

D26 PJDLC05 — LP9 DLW21HN900SQ2L — 15 USBP3+ / 15 USBP3- — USBVCC3 — C160 *47P, C185 *47P — CON20 USB usb-020173mr004s582zl-c2-4p-l-h

D20 PJDLC05 — LP12 DLW21HN900SQ2L — 15 USBP5- / 15 USBP5+ — USBVCC5 — C7 *47P, C8 *47P — CON14 USB

Vertical Type

D22 PJDLC05 — LP7 DLW21HN900SQ2L — 15 USBP1- / 15 USBP1+ — USBVCC7 — C40 *47P, C43 *47P — 85204-0400L CON8

To USB wire

1/11 stuff LP11,LP10,LP9,LP0 for EMI

PAD8 *EMIPAD142X91, PAD14 *EMIPAD142X91, PAD11 *EMIPAD142X91, PAD12 *EMIPAD142X91, PAD15 *EMIPAD142X91

PAD13 *EMIPAD138X98, PAD10 *EMIPAD142X91, PAD9 *EMIPAD142X91, PAD7 *EMIPAD142X91, PAD16 *EMIPAD177X106

4/15 remove BOT PAD for TV

H10 H-C307D118P2, H8 H-C307D118P2, H11 h-tc307be335x40HC307D118P2, H9 H-C307D118P2, H13 H-C307D118PT

H15 H-C307D118P2, H17 h-tc307be283x30HC307D118P2, H18 h-tc307be307x33HC307D118P2, H21 H-C307D118P2, H25 H-C307D118P2

H24 H-C307D118P2, H29 H-C307D118P2, H26 H-C307D118P2, H27 H-C307D118P2

Check Pin Define

CON9 — 88502-2401-24P-L

29 MY15 MY15 1, 29 MY13 MY13 2, 29 MY12 MY12 3, 29 MY0 MY0 4, 29 MY2 MY2 5, 29 MY11 MY11 6, 29 MY14 MY14 7, 29 MY10 MY10 8, 29 MY9 MY9 9, 29 MY8 MY8 10, 29 MY7 MY7 11, 29 MY6 MY6 12, 29 MY5 MY5 13, 29 MY3 MY3 14, 29 MY1 MY1 15, 29 MY4 MY4 16, 29 MX5 MX5 17, 29 MX6 MX6 18, 29 MX0 MX0 19, 29 MX3 MX3 20, 29 MX7 MX7 21, 29 MX1 MX1 22, 29 MX4 MX4 23, 29 MX2 MX2 24

KeyBoard Connector

Bot contact???

24 — 1

CP7 220Px4: MY15 MY13 MY12 MY0

CP8 220Px4: MY2 MY11 MY14 MY10

CP9 220Px4: MY9 MY8 MY7 MY6

CP10 220Px4: MY5 MY3 MY1 MY4

CP11 220Px4: MX5 MX6 MX0 MX3

CP12 220Px4: MX7 MX1 MX4 MX2

3VPCU

RP8 10KX8: MY4 MY1 MY3 MY5 — MY9 MY8 MY7 MY6

RP9 10KX8: MX2 MX4 MX1 MX7 — MX5 MX6 MX0 MX3

RP7 10KX8: MY10 MY14 MY11 MY2 — MY15 MY13 MY12 MY0

H19 H-C315D177P2, H20 H-C315I217D177P2, H22 H-C315D177P2, H23 H-C315I217D177P2

4/11 for 1-seg TV

H31 H-TC39BC256D39P2, H32 H-TC39BC256D39P2

NPTH hole

H28 h-c95d95n, H7 h-c95d95n, H30 H-C98D98N

PAD17 *PAD-C236NPT, PAD18 *PAD-C236NPT

2/12 for ME copper contact

H16 H-TC39BC295D39P2, H14 H-TC39BC295D39P2

1/11 for USB wire GND

H12 h-tc217bc307d118p2

H33 H-C405D244P2

Quanta Computer Inc.

PROJECT : ES2

Size	Document Number	Rev
	KEYBOARD/USB/SCREW	A

Date: Thursday, May 24, 2007 Sheet 28 of 35

1/15 use Winbond chip as main source, since NSC will be EOL.
using AJ875410F42 (Winbond P/N: 87541VDG/K2)
NSC/Winbond AJ875410F34 is going to EOL

If VBAT is not used, it is connected to AVCC,
otherwise connected to VCCRTC.

12/18 remove 1024K EEPROM
to save space

87541VDG/K2

U27

Strapping Pin

HWPG_1 R154 10K
BA2 R325 *10K
BA3 R324 *10K
BA5 R323 10K
BA1 R322 *10K
NBSWON# R393 10K
WLSW R395 *10K
BATLOW# R361 10K

1/2 BA19 this support 1024KB EEPROM

1/18 winbond FAE suggest placed close to 87541(

C533 10U_6.3V

Model ID

MID
3 2 1
0 0 0:
0 0 1:
0 1 0: Sharp INT_VGA
0 1 1:

Stuff Socket in BOM for debug during pilot run
DGP32000311 socket, no stuff in B-test
AKE148AP516

U22
PM39LV040-70JCE

	I/O Address	
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

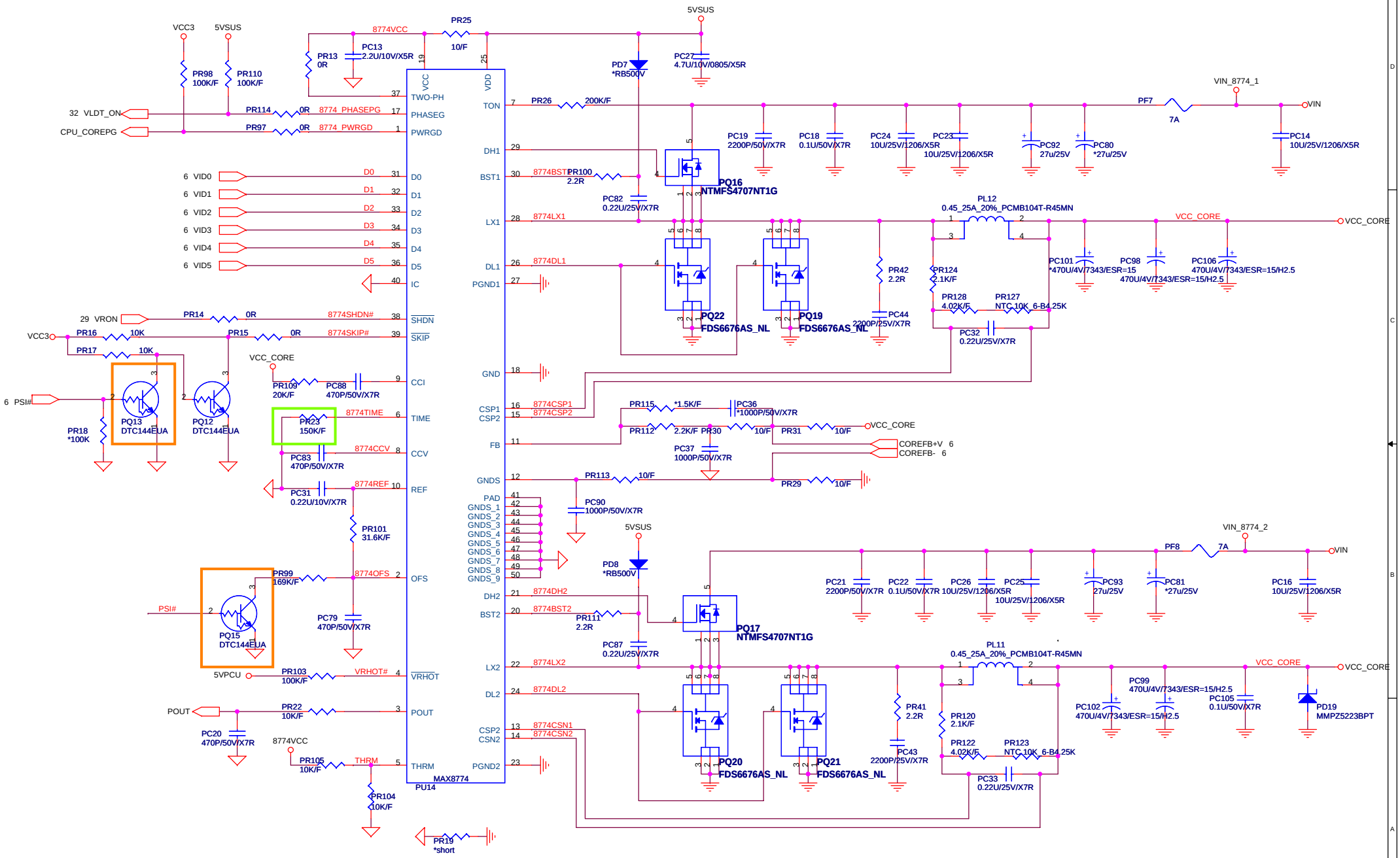
BA2 : BADDR0
BA3 : BADDR1

Environment	ENV0(BA0)	ENV1(BA1)	TRIS(BA4)
IRE	0	0	0
OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

BA0 : ENV0
BA1 : ENV1
BA4 : TRIS(If =1 will tristate all I/O pins)
BA5 : SHBM(If =1 Enable share host BIOS memory)

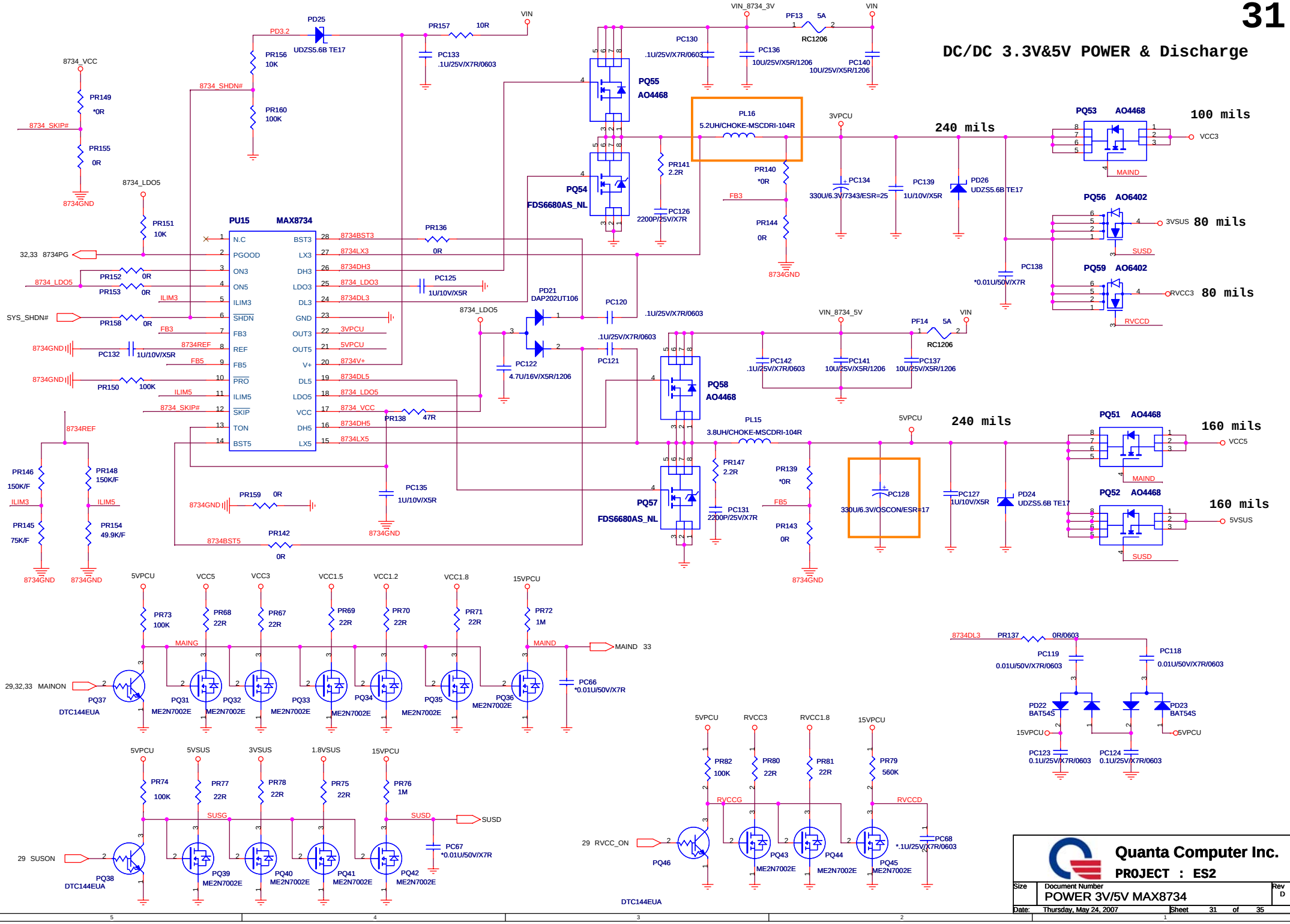
1/22
TXC BG332768909 KW3S, supply tight, as main source
SEG BG332768224 try it in A-test 2nd source, supply good

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: EC PCU87541/FLASH ROM	Rev D
Date: Thursday, May 24, 2007	Sheet 29 of 35	

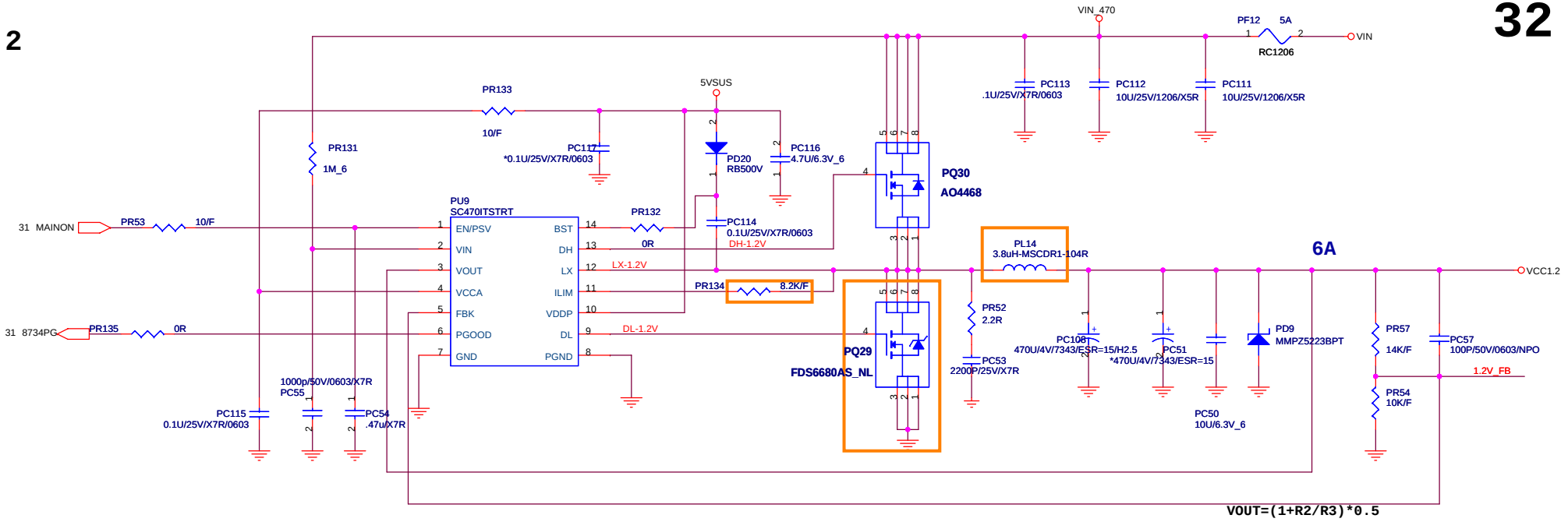


Quanta Computer Inc.			
PROJECT : ES2			
Size	Document Number		Rev
	POWER CPU CORE MAX8774		D
Date: Thursday, May 24, 2007	Sheet 30 of 35		

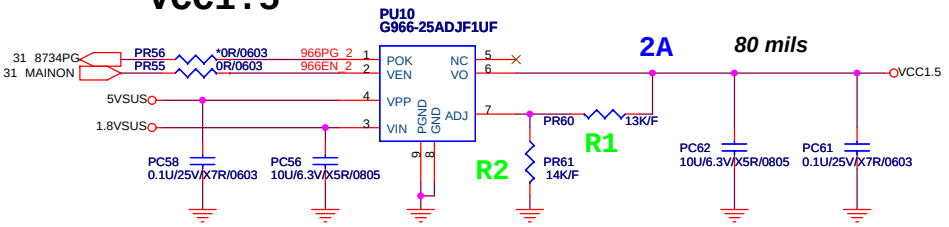
DC/DC 3.3V&5V POWER & Discharge



VCC1.2

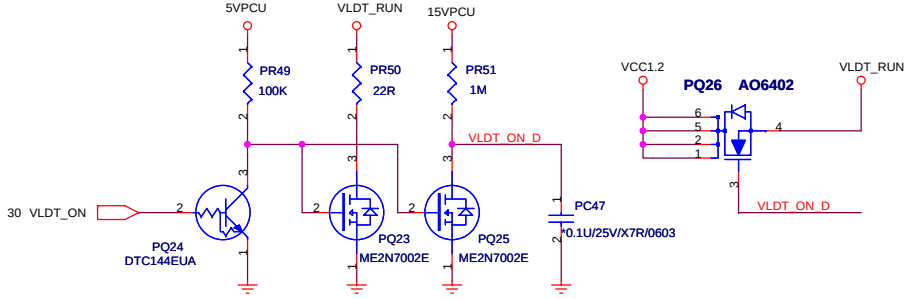


VCC1.5



Vout =0.8*(1+R1/R2)
= 0.8* (1+13K/14K)
= 1.54V

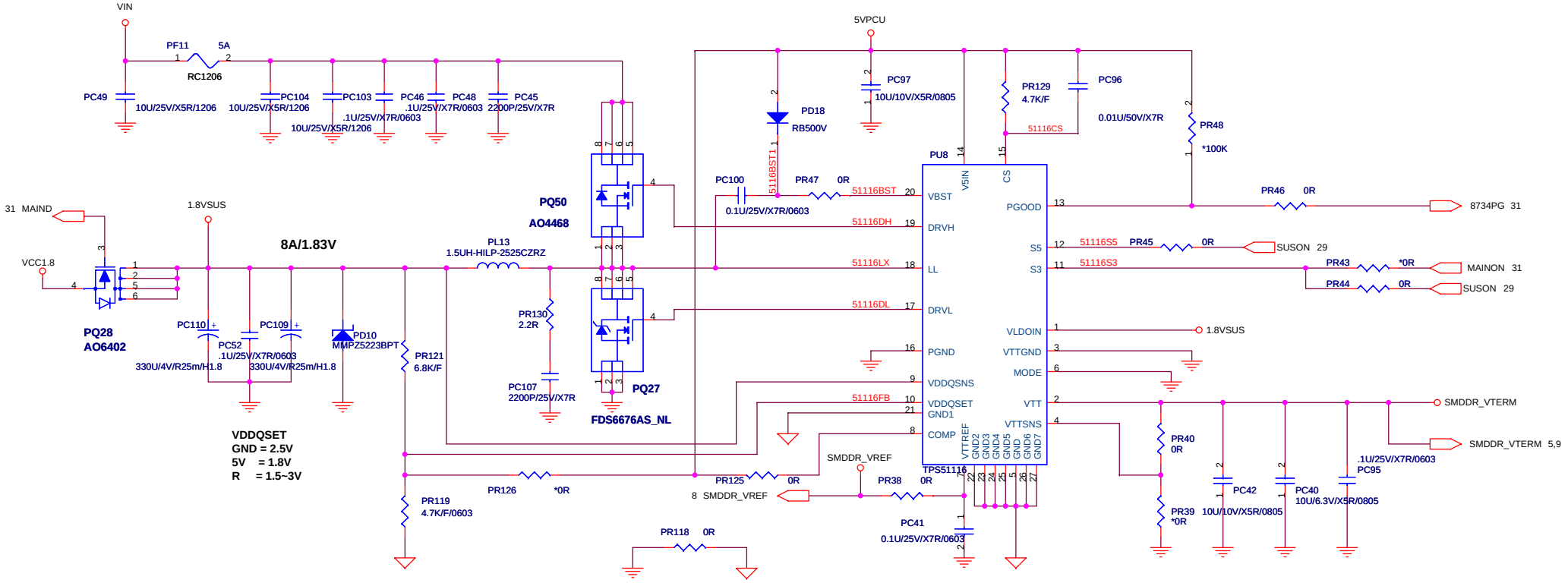
VLDT_RUN



Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	POWER 1.2V/1.5V/2.5V	D
Date: Thursday, May 24, 2007	Sheet 32 of 35	

1.8VSUS & VTERM(DDR2) & VCC1.8

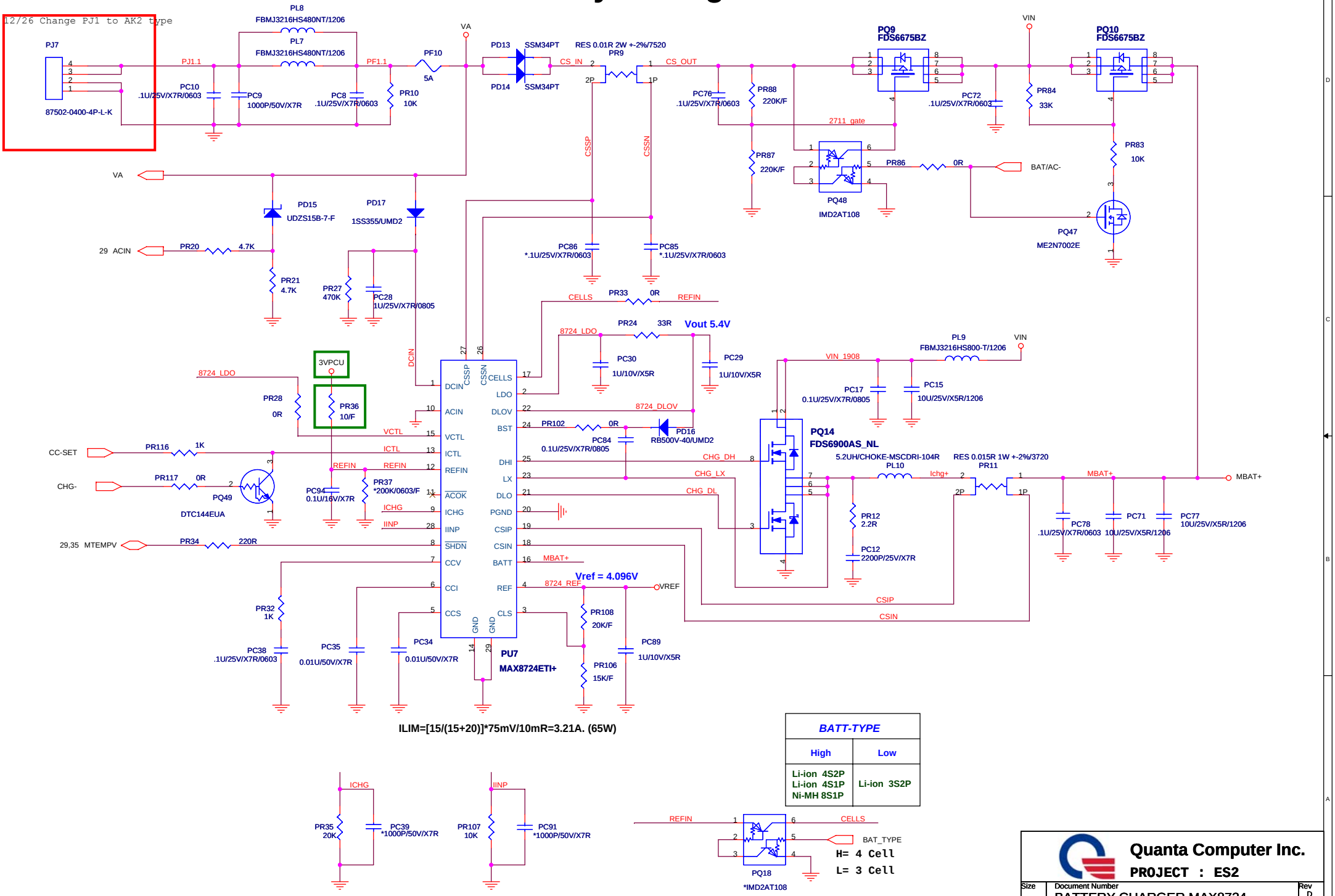


RVCC1.8

Vout =1.25(1+R1/R2)
= 1.25 (1+4.7K/10K)
= 1.83V

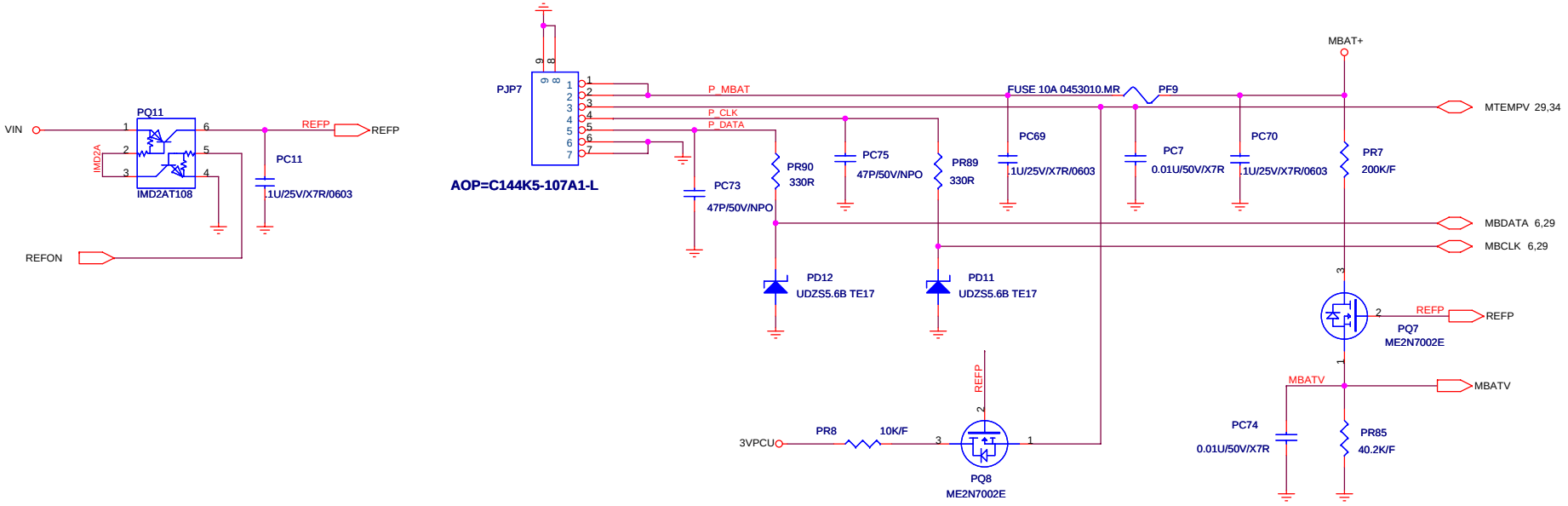
Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: POWER 1.8VSUS/DDR VTERM	Rev D
Date: Thursday, May 24, 2007	Sheet 33 of 35	

Battery Charger



Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: BATTERY CHARGER MAX8724	Rev D
Date: Thursday, May 24, 2007	Sheet 34 of 35	

Battery Connector



MTEMPV voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :

16.8V*40.2/(200+40.2)= 2.812V

12.0V*40.2/(200+40.2)= 2.008V

8.0V*40.2/(200+40.2)= 1.34V

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: BATTERY CONNECTOR	Rev: D
Date: Thursday, May 24, 2007	Sheet 35 of 35	