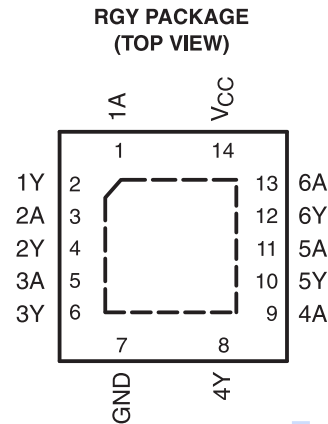
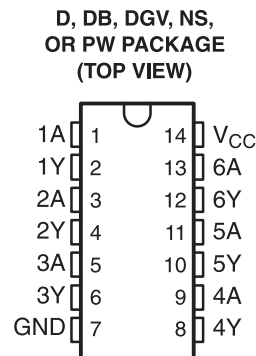


## HEX BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

### FEATURES

- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max  $t_{pd}$  of 2.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17



### DESCRIPTION/ORDERING INFORMATION

This hex buffer/driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC07ARGYR	LC07A
		Tube of 50	SN74LVC07AD	LVC07A
	SOIC – D	Reel of 2500	SN74LVC07ADR	
		Reel of 250	SN74LVC07ADT	
	SOP – NS	Reel of 2000	SN74LVC07ANSR	LVC07A
	SSOP – DB	Reel of 2000	SN74LVC07ADBR	LC07A
	TSSOP – PW	Tube of 90	SN74LVC07APW	LC07A
		Reel of 2000	SN74LVC07APWR	
		Reel of 250	SN74LVC07APWT	
TVSOP – DGV	Reel of 2000	SN74LVC07ADGVR	LC07A	

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

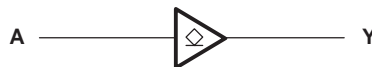
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE  
(EACH BUFFER/DRIVER)**

INPUT A	OUTPUT Y
H	H
L	L

**LOGIC DIAGRAM, EACH BUFFER/DRIVER (POSITIVE LOGIC)**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Output voltage range	-0.5	6.5	V
$I_{IK}$	Input clamp current		-50	mA
		$V_I < 0$		
$I_{OK}$	Output clamp current		-50	mA
		$V_O < 0$		
$I_O$	Continuous output current		±50	mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance	D package <sup>(3)</sup>	86	°C/W
		DB package <sup>(3)</sup>	96	
		DGV package <sup>(3)</sup>	127	
		NS package <sup>(3)</sup>	76	
		PW package <sup>(3)</sup>	113	
		RGY package <sup>(4)</sup>	47	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.65	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.3 \times V_{CC}$	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	5.5	V
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
		$V_{CC} = 4.5\text{ V}$	24	
$T_A$	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	1.65 V to 5.5 V			0.2	V
	$I_{OL} = 4\ \text{mA}$	1.65 V			0.45	
	$I_{OL} = 12\ \text{mA}$	2.3 V			0.7	
		2.7 V			0.4	
	$I_{OL} = 24\ \text{mA}$	3 V			0.55	
$I_I$	$V_I = 5.5\text{ V or GND}$	3.6 V			±5	μA
$I_{off}$	$V_I$ or $V_O = 5.5\text{ V}$	0 V			±10	μA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			10	μA
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	2.7 V to 3.6 V			500	μA
$C_i$	$V_I = V_{CC}$ or GND	3.3 V		5		pF

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#) through [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1	5.6	1	3.4	3.3		1	3.6	1	2.6	ns

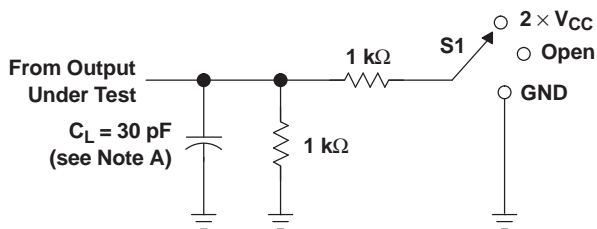
## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per buffer/driver	$f = 10\text{ MHz}$	1.8	2	2.5	3.78	pF

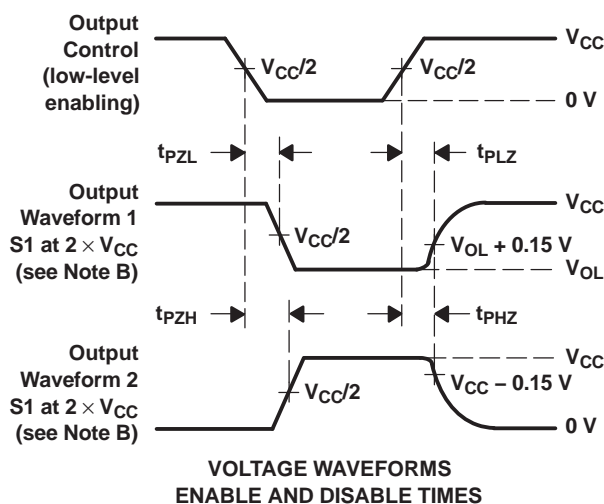
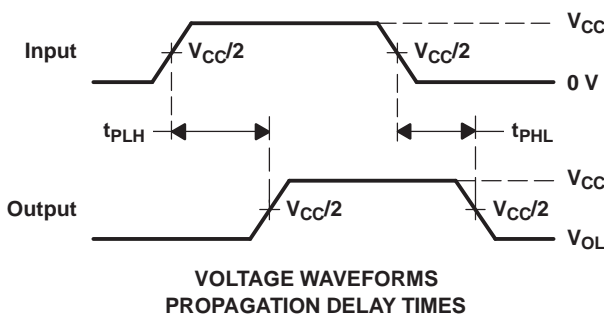
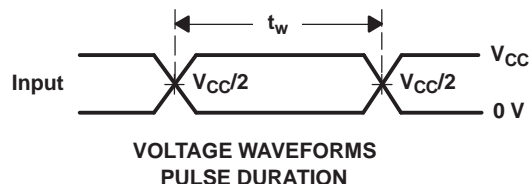
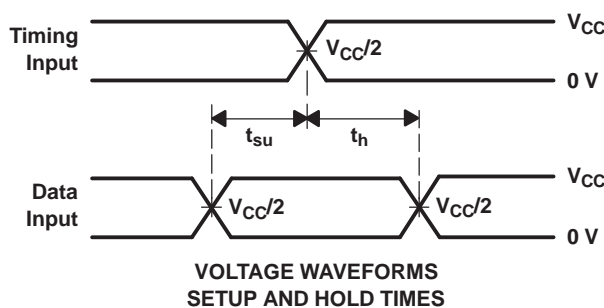
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



LOAD CIRCUIT

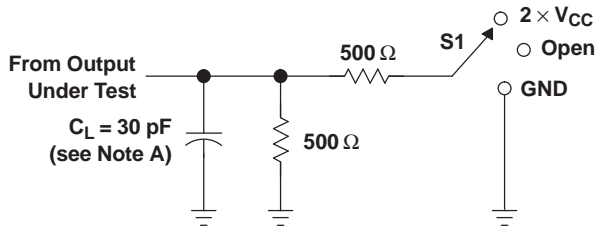
TEST	S1
$t_{PZL}$ (see Note F)	$2 \times V_{CC}$
$t_{PLZ}$ (see Note G)	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	$2 \times V_{CC}$



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{PZL}$  is measured at  $V_{CC}/2$ .  
 G.  $t_{PLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .  
 H. All parameters and waveforms are not applicable to all devices.

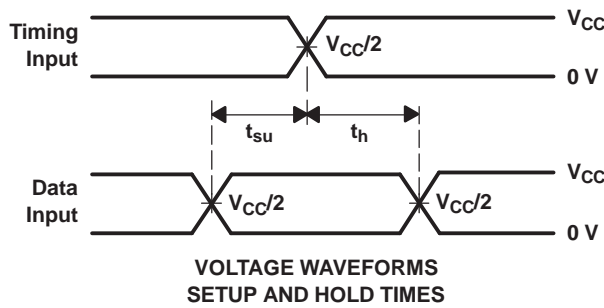
Figure 1. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

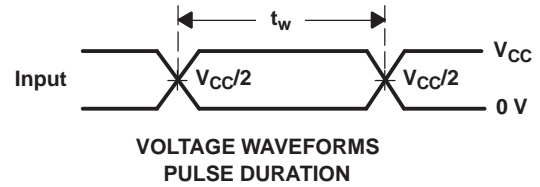


**LOAD CIRCUIT**

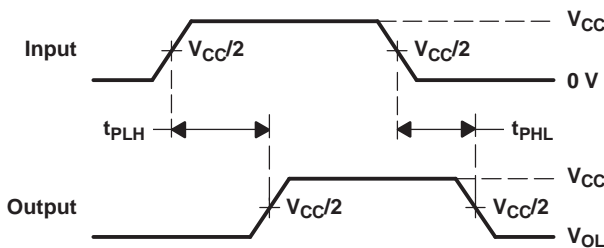
TEST	S1
$t_{PZL}$ (see Note F)	$2 \times V_{CC}$
$t_{PLZ}$ (see Note G)	$2 \times V_{CC}$
$t_{PHZ}/t_{PHZ}$	$2 \times V_{CC}$



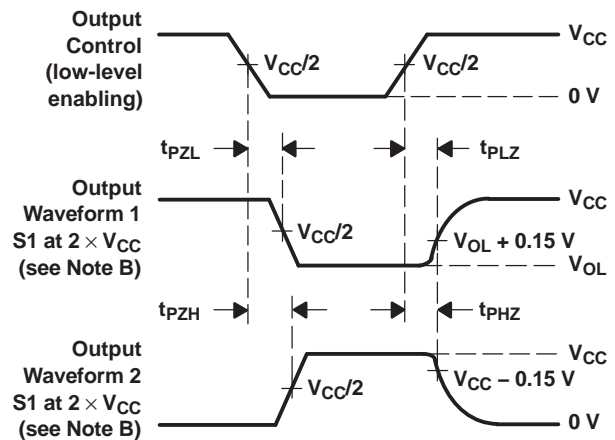
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



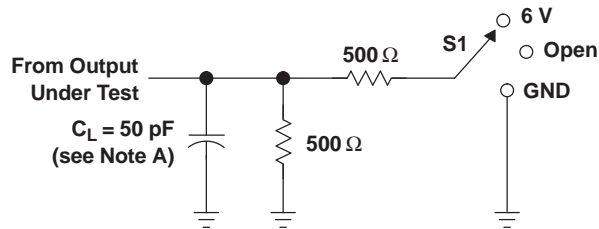
**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{PZL}$  is measured at  $V_{CC}/2$ .  
 G.  $t_{PLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ and } 3.3 \text{ V} \pm 0.3 \text{ V}$

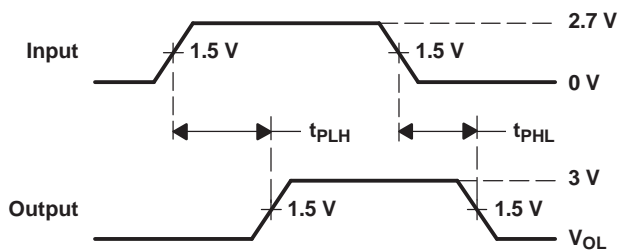


LOAD CIRCUIT

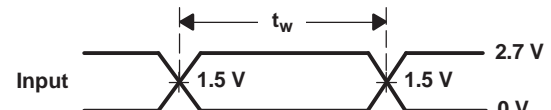
TEST	S1
$t_{pZL}$ (see Note F)	6 V
$t_{pLZ}$ (see Note G)	6 V
$t_{PHZ}/t_{PZH}$	6 V



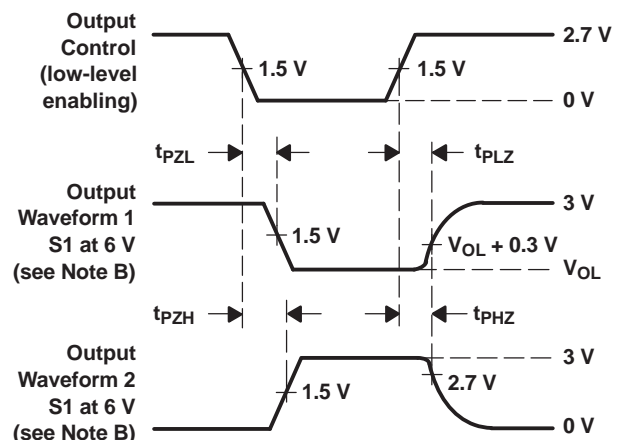
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION



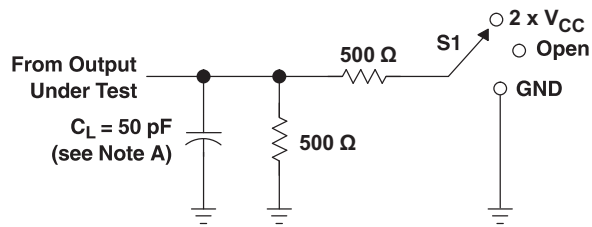
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .
  - F.  $t_{pZL}$  is measured at 1.5 V.
  - G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.3 \text{ V}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

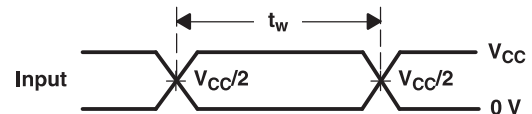
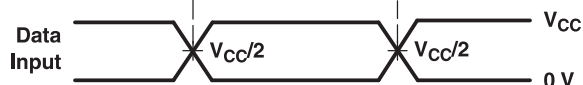
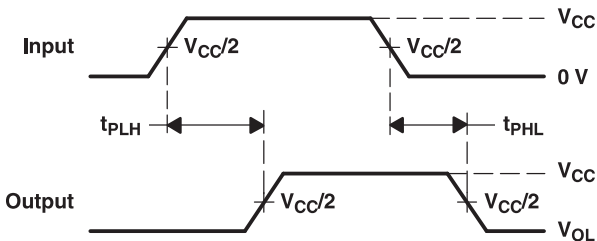
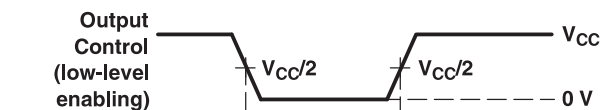
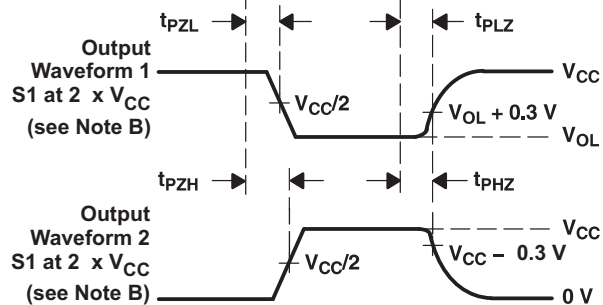
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$$



LOAD CIRCUIT

TEST	S1
$t_{PZL}$ (see Note F)	$2 \times V_{CC}$
$t_{PLZ}$ (see Note G)	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	$2 \times V_{CC}$

VOLTAGE WAVEFORMS  
PULSE DURATIONVOLTAGE WAVEFORMS  
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal connections such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal connections such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
- F.  $t_{PZL}$  is measured at  $V_{CC}/2$ .
- G.  $t_{PLZ}$  is measured at  $V_{OL} + 0.3\text{ V}$ .
- H. All parameters and waveforms are not applicable to all devices.

### Figure 4. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC07AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC07APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVC07APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LVC07ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN74LVC07A :**

- Automotive: [SN74LVC07A-Q1](#)
- Enhanced Product: [SN74LVC07A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC07ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC07ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC07ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC07ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC07APWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVC07ARGYR	QFN	RGY	14	1000	180.0	12.4	3.85	3.85	1.35	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC07ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LVC07ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74LVC07ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LVC07ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LVC07APWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74LVC07ARGYR	QFN	RGY	14	1000	190.5	212.7	31.8

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

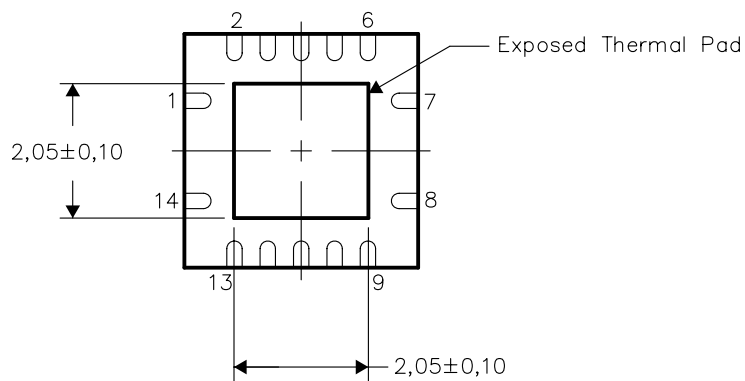
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BA.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



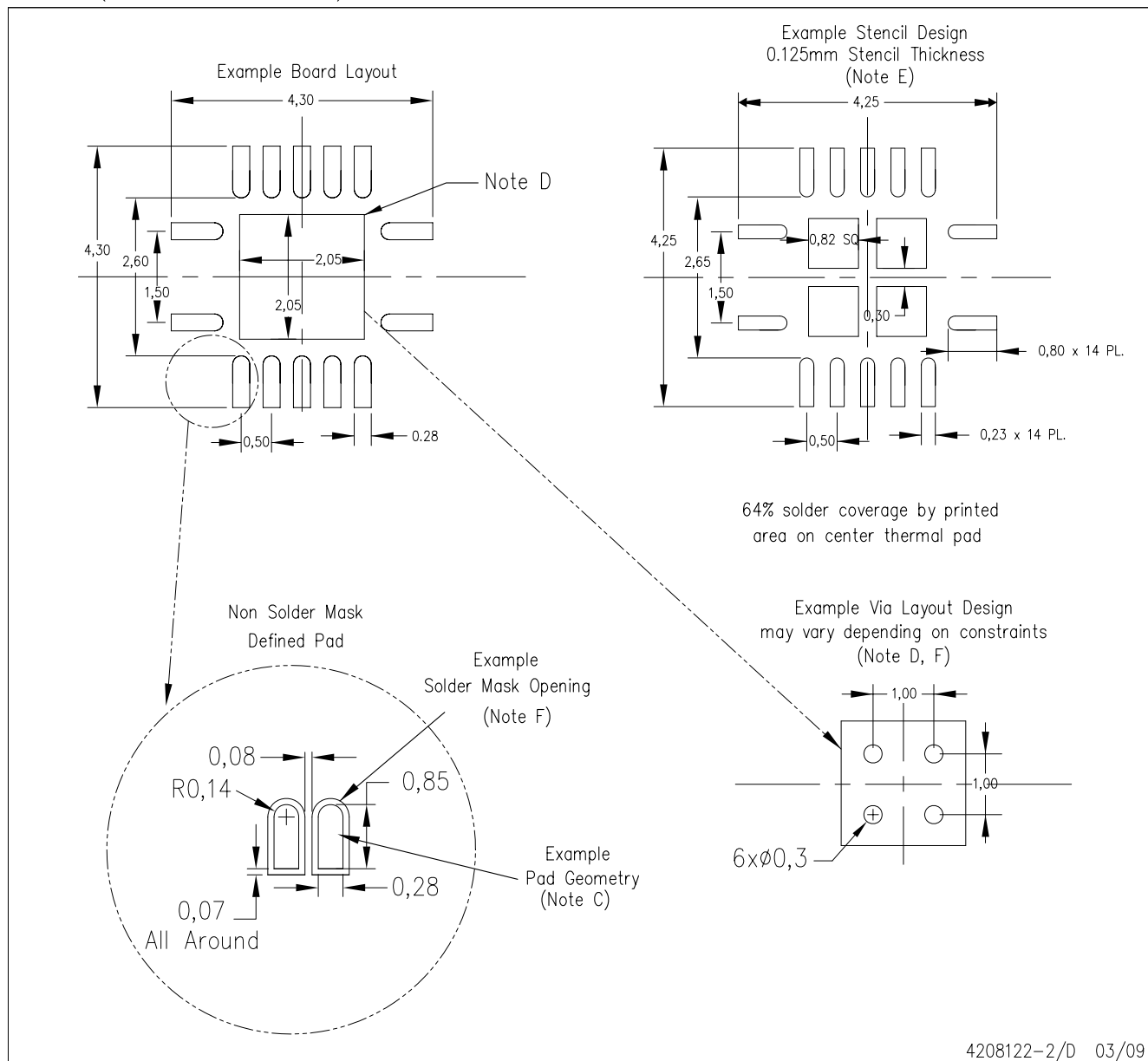
Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions



## RGY (R-PQFP-N14)





- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  -  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

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