INTERSIL

2N6660-1
n-Channel Enhancement-mode Vertical Power MOSFET

FEATURES

- *High speed, high current switching*
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- Simple DC biasing
- Extended safe operating area
- Inherently temperature stable
- Typical t_{on} and t_{off} < 5ns

APPLICATIONS

- *Switching power supplies*
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers
- High frequency linear amplifiers

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ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Drain-source Voltage
- IVN6660 ..... 60V
- IVN6661 ..... 90V

Drain-gate Voltage
- IVN6660 ..... 60V
- IVN6661 ..... 90V

Continuous Drain Current (see note 1) 2.0A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 8.33W

Linear Derating Factor ..... 67mW/°C
Operating Junction
- Temperature Range ..... –55 to +150°C

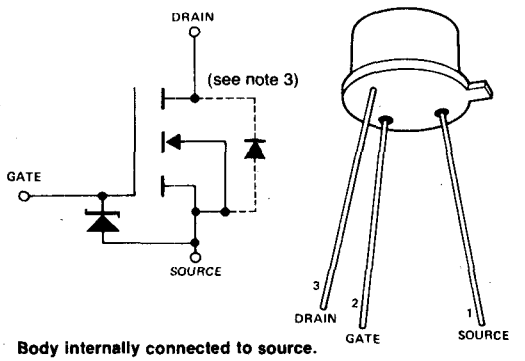
Storage Temperature Range ..... –55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $r_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

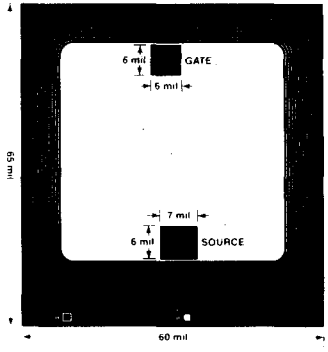
Note 3. The Drain-source diode is an integral part of the MOSFET structure.

SCHEMATIC DIAGRAM (OUTLINE DWG. TO-39)



Body internally connected to source.
Drain common to case.

CHIP TOPOGRAPHY

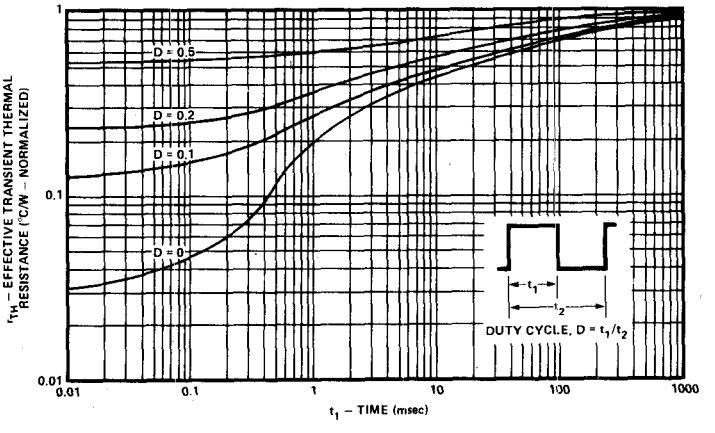


ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

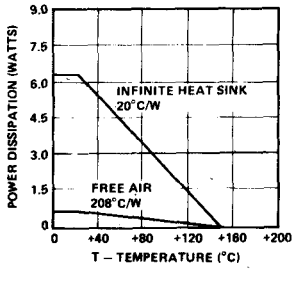
		CHARACTERISTIC		IVN6660 MIN	IVN6660 TYP	IVN6660 MAX	IVN6661 MIN	IVN6661 TYP	IVN6661 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	V_{GS} = 0, I_D = 10μA	
2				60			90				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
5						500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C	(Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7						500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.4		V	V_{GS} = 5V, I_D = 0.1 A	
11					1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 A	
12					0.9			1.3			V_{GS} = 10V, I_D = 0.5 A	
13					2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0 A	
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	V_{GS} = 10V, I_D = 1.0 A	
15		$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0 A	f = 1KHz
16		g_{fs}	Forward Transconductance	170	250		170	250		mΩ	V_{DS} = 24V, I_D = 0.5 A	
17	DYNAMIC	C_{iss}	Input Capacitance			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
18		C_{ds}	Drain-Source Capacitance			40			40		V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
19		C_{rss}	Reverse Transfer Capacitance			10			10		V_{GS} = 0, V_{DS} = 0, f = 1.0MHz	
20						35			35			
21		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns		
22		t_r	Rise Time		2	5		2	5			
23		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle. **Note 2.** Sample test.

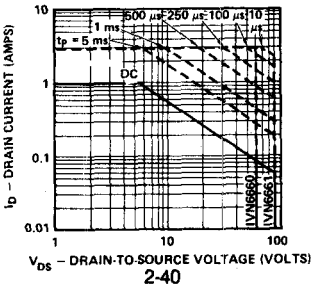
THERMAL RESPONSE



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION Tc = 25°C



BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE