

# BLF6G13L-250P; BLF6G13LS-250P

Power LDMOS transistor

Rev. 3 — 14 October 2011

Product data sheet

## 1. Product profile

### 1.1 General description

250 W LDMOS power transistor intended for CW applications at a frequency of 1.3 GHz.

**Table 1. Test information**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $I_{Dq} = 100\text{ mA}$ ; in a class-AB production test circuit.

Mode of operation	f (GHz)	V <sub>DS</sub> (V)	P <sub>L(1dB)</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)
CW	1.3	50	250	17	56

### 1.2 Features and benefits

- Typical CW performance at a frequency of 1.3 GHz, a supply voltage of 50 V, an  $I_{Dq}$  of 100 mA:
  - ◆ Output power = 250 W
  - ◆ Power gain = 17 dB
  - ◆ Efficiency = 56 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

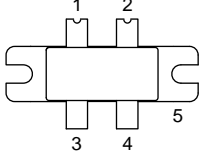
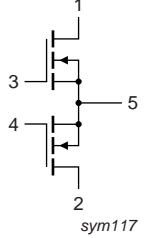
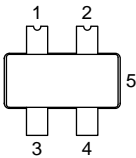
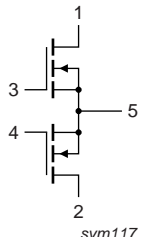
### 1.3 Applications

- Industrial, scientific and medical applications



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF6G13L-250P (SOT1121A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF6G13LS-250P (SOT1121B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G13L-250P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF6G13LS-250P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	100	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$I_D$	drain current		-	42	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 85\text{ °C}; P_L = 250\text{ W}$	0.26	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.4\text{ mA}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 235\text{ mA}$	1.4	1.8	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	-	21	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	240	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 120\text{ mA}$	-	1	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 4.75\text{ A}$	-	200	-	$\text{m}\Omega$

**Table 7. RF characteristics**

Mode of operation: CW;  $f = 1.3\text{ GHz}$ ; RF performance at  $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified, in a class-AB production test circuit.

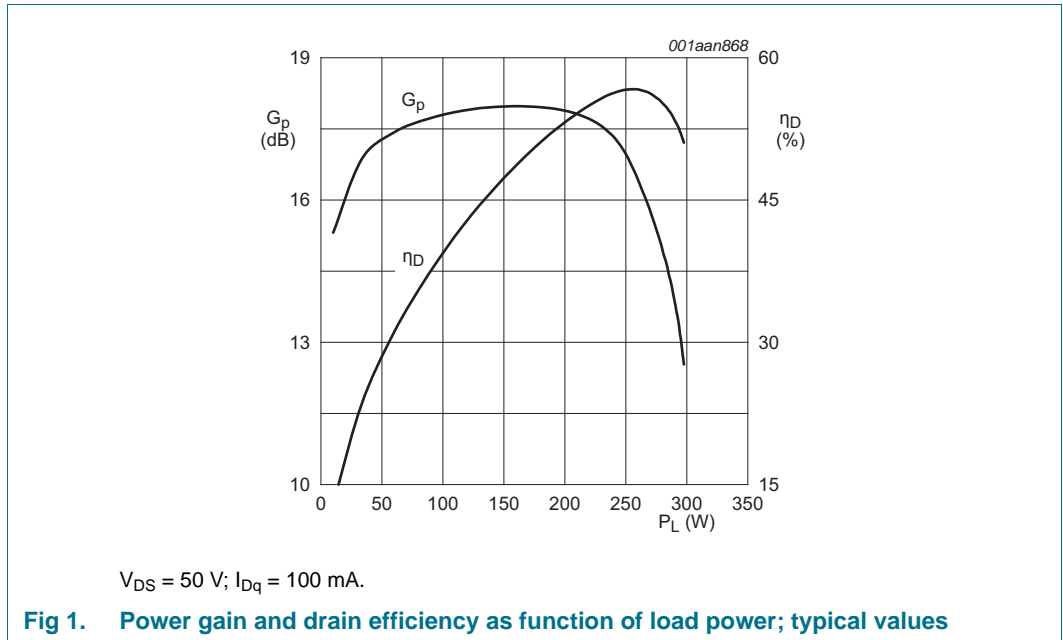
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_L$	output power		250	-	-	W
$V_{DS}$	drain-source voltage	$P_L = 250\text{ W}$	-	-	50	V
$G_p$	power gain	$P_L = 250\text{ W}$	15	17	-	dB
$RL_{in}$	input return loss	$P_L = 250\text{ W}$	-	-30	-20	dB
$\eta_D$	drain efficiency	$P_L = 250\text{ W}$	52	56	-	%

### 6.1 Ruggedness in class-AB operation

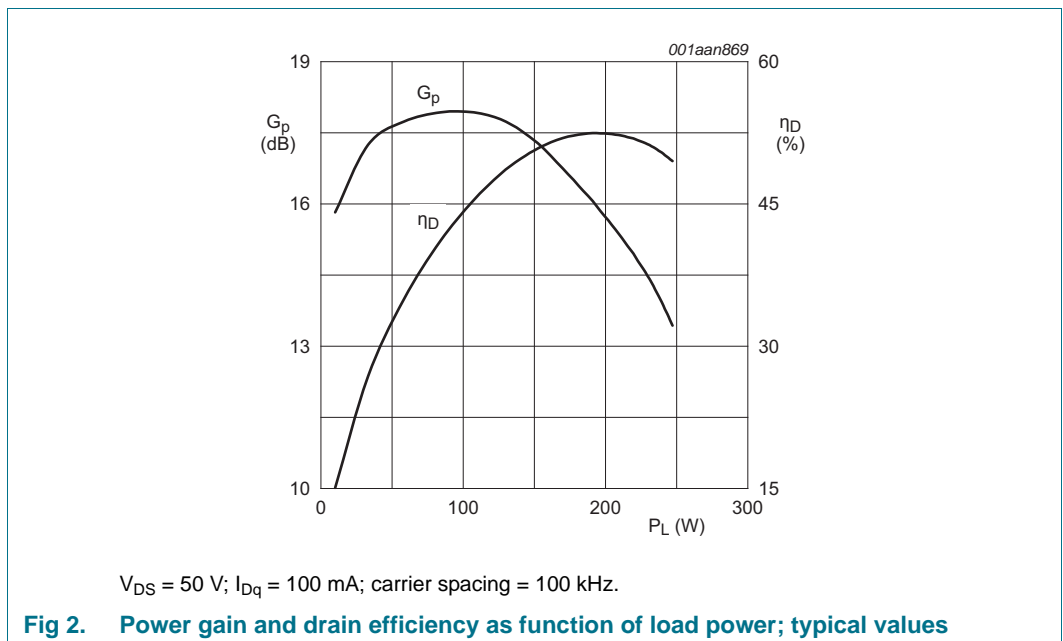
The BLF6G13L-250P and BLF6G13LS-250P are capable of withstanding a load mismatch corresponding to  $VSWR = 5 : 1$  through all phases under the following conditions:  $V_{DS} = 50\text{ V}; I_{Dq} = 100\text{ mA}; P_L = 250\text{ W}; f = 1.3\text{ GHz}$ .

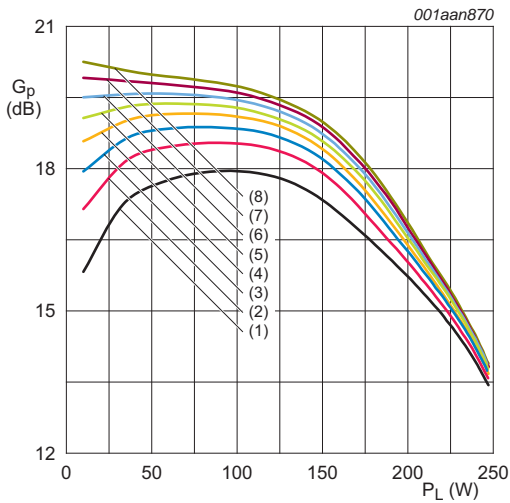
**7. Application information**

**7.1 CW**



**7.2 2-Carrier CW**

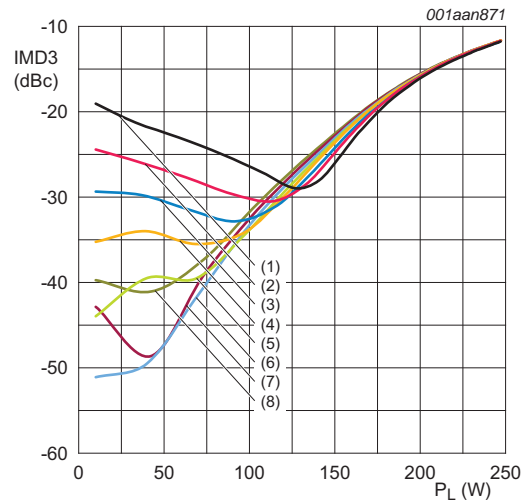




$V_{DS} = 50\text{ V}$ ;  $f = 1300\text{ MHz}$ ; carrier spacing = 100 kHz.

- (1)  $I_{Dq} = 100\text{ mA}$
- (2)  $I_{Dq} = 300\text{ mA}$
- (3)  $I_{Dq} = 500\text{ mA}$
- (4)  $I_{Dq} = 700\text{ mA}$
- (5)  $I_{Dq} = 900\text{ mA}$
- (6)  $I_{Dq} = 1100\text{ mA}$
- (7)  $I_{Dq} = 1300\text{ mA}$
- (8)  $I_{Dq} = 1500\text{ mA}$

**Fig 3. Power gain as a function of load power; typical values**



$V_{DS} = 50\text{ V}$ ;  $f = 1300\text{ MHz}$ ; carrier spacing = 100 kHz.

- (1)  $I_{Dq} = 100\text{ mA}$
- (2)  $I_{Dq} = 300\text{ mA}$
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- (7)  $I_{Dq} = 1300\text{ mA}$
- (8)  $I_{Dq} = 1500\text{ mA}$

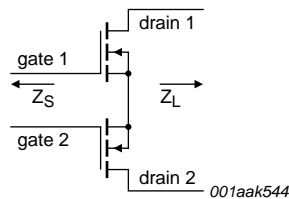
**Fig 4. Third order intermodulation distortion as a function of load power; typical values**

### 7.3 Impedance information

**Table 8. Typical impedance**

Typical values valid per section unless otherwise specified.

f MHz	$Z_S$ $\Omega$	$Z_L$ optimized for $G_p$ $\Omega$	$Z_L$ optimized for $\eta_D$ $\Omega$
1200	$3.03 - j8.15$	$2.03 - j0.25$	$1.46 - j0.47$
1300	$4.06 - j9.52$	$1.67 - j0.92$	$1.19 - j0.95$
1400	$7.00 - j9.61$	$1.50 - j1.48$	$1.22 - j1.49$



**Fig 5. Definition of transistor impedance**

## 7.4 Circuit information

**Table 9. List of components**

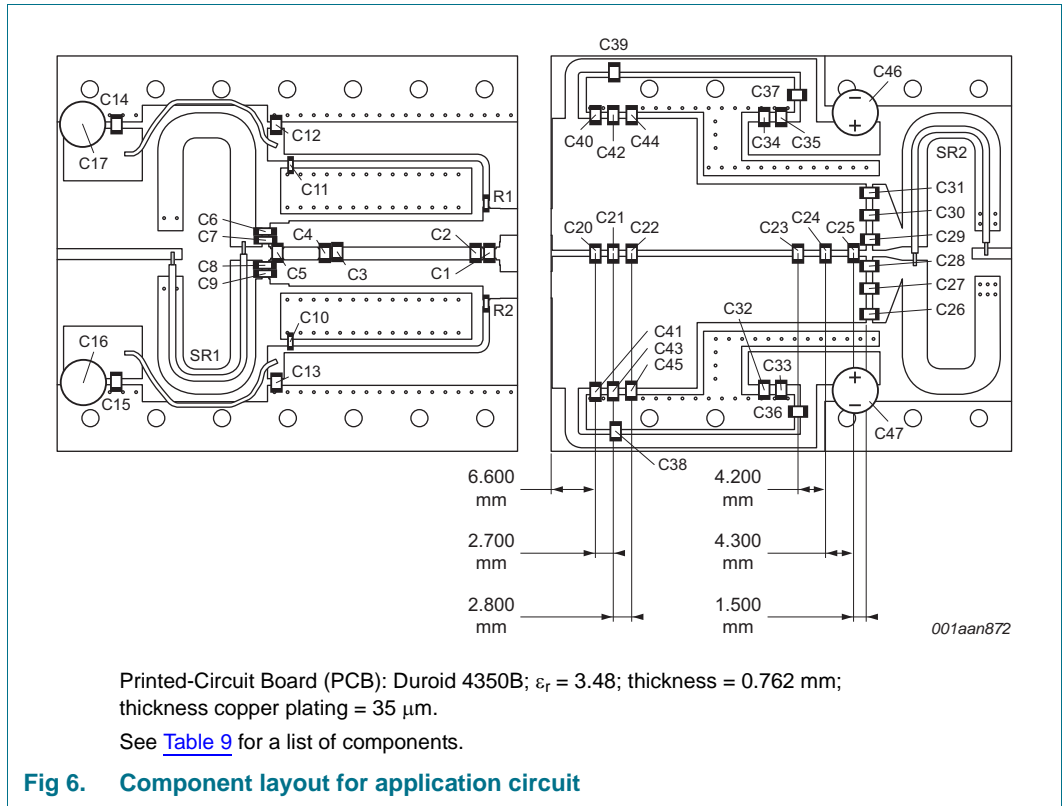
For application circuit see [Figure 6](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	1.9 pF	[1]
C3, C4	multilayer ceramic chip capacitor	4.7 pF	[1]
C5	multilayer ceramic chip capacitor	10 pF	[1]
C6, C7, C8, C9, C10, C11, C38, C39	multilayer ceramic chip capacitor	56 pF	[1]
C12, C13	multilayer ceramic chip capacitor	100 pF	[2]
C14, C15, C32, C34	multilayer ceramic chip capacitor	1 nF	[2]
C16, C17	electrolytic capacitor	10 $\mu$ F; 50 V	220 X5R
C20, C21, C22, C23	multilayer ceramic chip capacitor	3.0 pF	[1]
C40, C41	multilayer ceramic chip capacitor	2.4 pF	[1]
C42, C43, C44, C45	multilayer ceramic chip capacitor	2.7 pF	[1]
C24	multilayer ceramic chip capacitor	0.8 pF	[1]
C25	multilayer ceramic chip capacitor	0.6 pF	[1]
C26, C27, C28, C29, C30, C31, C33, C35	multilayer ceramic chip capacitor	100 pF	[1]
C36, C37	multilayer ceramic chip capacitor	20 nF	[3]
C46, C47	electrolytic capacitor	100 $\mu$ F; 63 V	
R1, R2	SMD resistor 0603	5.1 $\Omega$	UT-141C-25-TP
SR1	COAX	25 $\Omega$	UT-141C-35-TP
SR2	COAX	35 $\Omega$	

[1] American Technical Ceramics type 800B or capacitor of same quality.

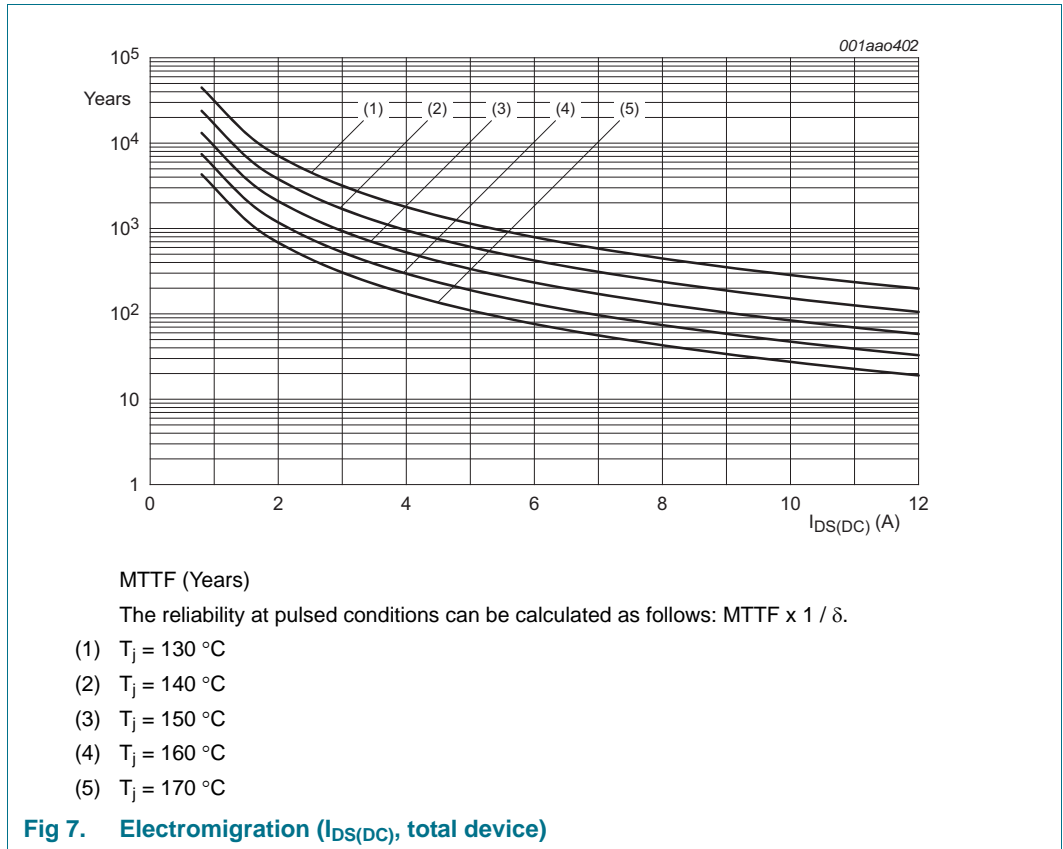
[2] American Technical Ceramics type 100B or capacitor of same quality.

[3] American Technical Ceramics type 200B or capacitor of same quality.



**8. Test information**

**8.1 Reliability**





9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1121A

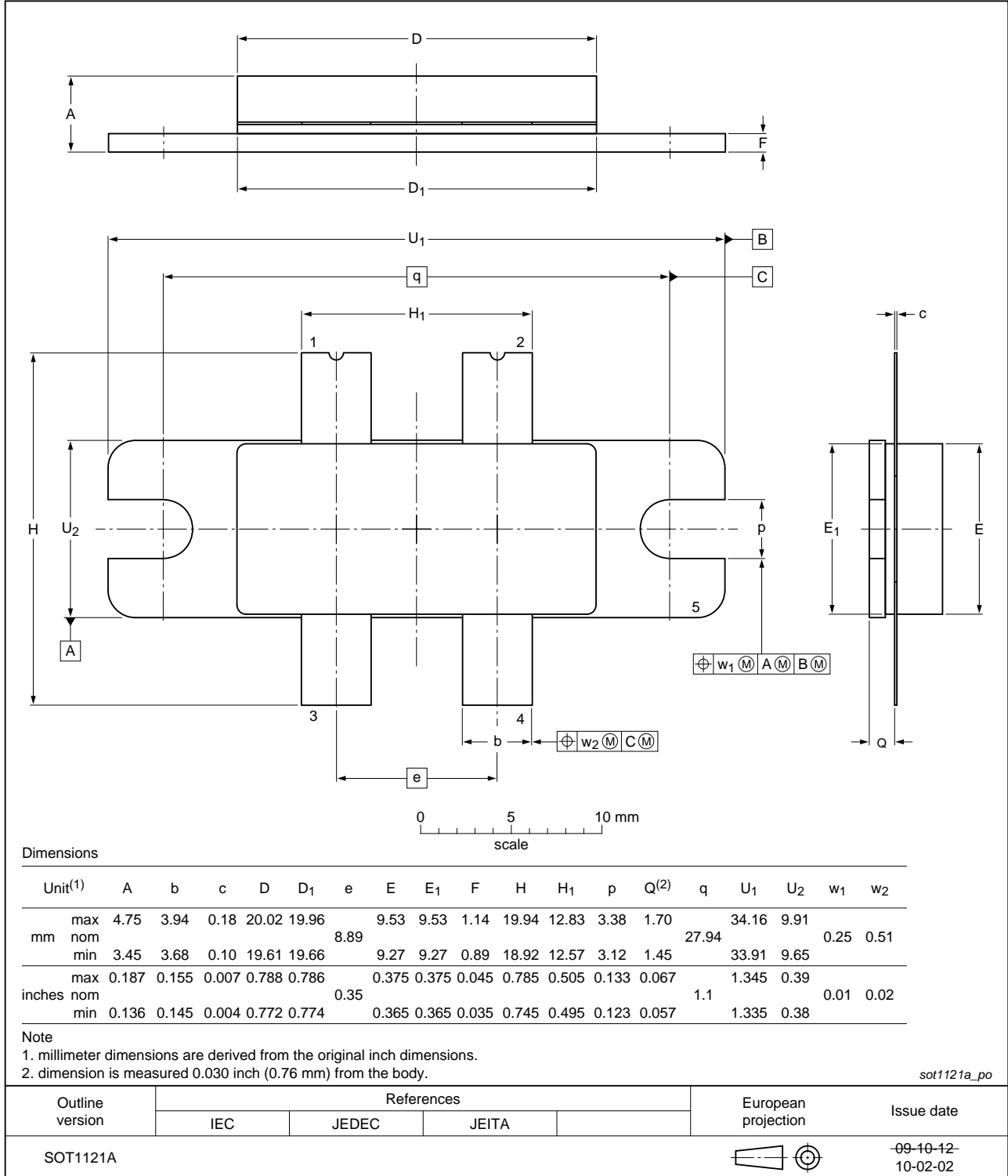


Fig 8. Package outline SOT1121A

Earless flanged LDMOST ceramic package; 4 leads

SOT1121B

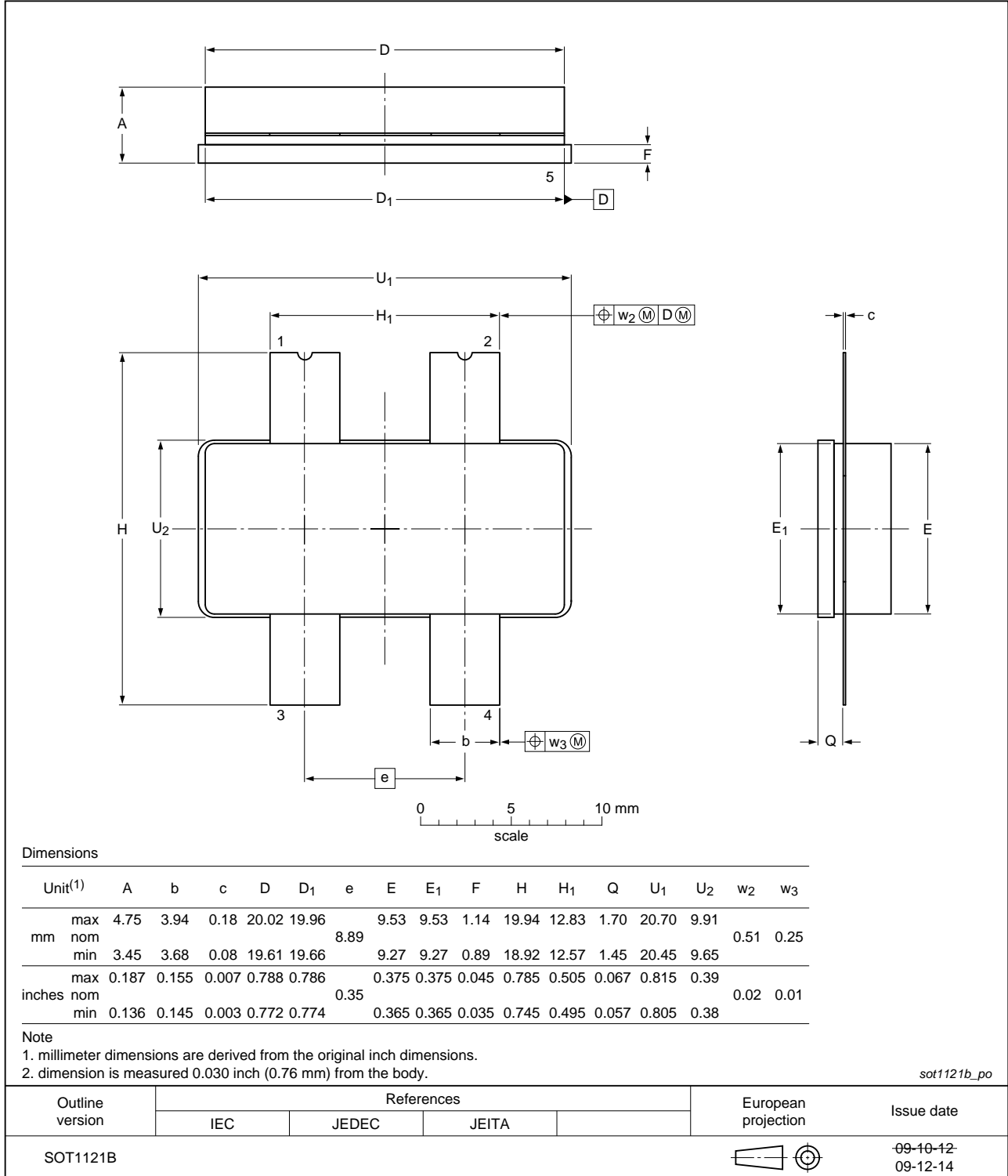


Fig 9. Package outline SOT1121B

## 10. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
MTTF	Mean Time To Failure
RF	Radio Frequency
SMD	Surface Mount Device
VSWR	Voltage Standing-Wave Ratio

## 12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G13L-250P_6G13LS-250P v.3	20111014	Product data sheet	-	BLF6G13L-250P_6G13LS-250P v.2
Modifications:		<ul style="list-style-type: none"> <li>• <a href="#">Table 6 on page 3</a>: Several values have been updated</li> <li>• <a href="#">Table 7 on page 3</a>: The minimum value for <math>\eta_D</math> has been updated</li> <li>• <a href="#">Section 8.1 on page 8</a>: This section has been added</li> </ul>		
BLF6G13L-250P_6G13LS-250P v.2	20110321	Objective data sheet	-	BLF6G13L-250P_6G13LS-250P v.1
BLF6G13L-250P_6G13LS-250P v.1	20101102	Objective data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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