The V850 Series of high-performance microcontrollers answers many different application system needs. It realizes superlatively low power consumption and low noise while offering high performance and a wide array of functions. The broad V850 product lineup provides optimum solutions for the next-generation systems of customers.
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Continuously evolving V850 Series through an expanding product lineup

**V850 Series Product Roadmap**

**High-end lineup**

- **V850E2 core**
  - Frequency: 200 to 400 MHz
- **V850E1 core**
  - Frequency: 150 MHz @ 215 MIPS
  - Memory size: ROM: ROM-less to 512 KB
  - RAM: 4 to 128 KB
  - PKG: 100 to 240 pins (QFP & FBGA)

**Middle-range lineup**

- **V850 core**
  - Frequency: 33 MHz @ 38 MIPS
  - Memory size: ROM: ROM-less to 640 KB
  - RAM: 4 to 48 KB
  - PKG: 100 to 144 pins (QFP & FBGA)

**Low-end lineup**

- **V850ES core**
  - Frequency: 20 MHz @ 29 MIPS
  - Memory size: ROM: 64 to 256 KB
  - RAM: 4 to 16 KB
  - PKG: 64 to 144 pins (QFP)

**ASSP lineup**

- **Inverter control**
- **DVC control**
- **Car audio control**
- **Power meter control**
- **Dashboard control**

- Frequency: 16 to 64 MHz
- Memory size: ROM: ROM-less to 640 KB
- RAM: 4 to 48 KB
- PKG: 64 to 257 pins (QFP & FBGA)

**Realization of low EMI noise**

- Frequency: 20 to 34 MHz
- Memory size: ROM: ROM-less to 640 KB
- RAM: 4 to 48 KB
- PKG: 100 to 144 pins (QFP & FBGA)

**High cost-performance**

- Frequency: 20 MHz
- Memory size: ROM: 64 to 256 KB
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**Roadmap/Features**

- **V850 Series Product Roadmap**
- Continuously evolving V850 Series through an expanding product lineup

**CPU core release completed**

- Product deployment under planning

**Standard lineups**

**Field-specific lineups**

**High-performance:** On-chip MEMC/DMA

**High cost-performance**

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**High cost-performance**

- Frequency: 20 MHz
- Memory size: ROM: 64 to 256 KB
- RAM: 4 to 16 KB
- PKG: 64 to 144 pins (QFP)
The V850 Series is suitable for various application fields and raises the commercial value of customer systems.

<table>
<thead>
<tr>
<th>Application</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automotive</td>
<td>Engines, dashboards, power steering, ABS</td>
</tr>
<tr>
<td>Audio</td>
<td>Car audio, portable audio, component stereo systems</td>
</tr>
<tr>
<td>Portable devices</td>
<td>PDA, IC recorders</td>
</tr>
<tr>
<td>Camera</td>
<td>DVC, DSC, SLR cameras</td>
</tr>
<tr>
<td>Computer peripherals</td>
<td>Laser-beam printers, inkjet printers, scanners, fax machines</td>
</tr>
<tr>
<td>Home appliances</td>
<td>Air conditioners, refrigerators, washing machines, microwave ovens</td>
</tr>
<tr>
<td>Industrial equipment</td>
<td>Industrial motors, control equipment, vending machines, power meters</td>
</tr>
<tr>
<td>Video and recording equipment</td>
<td>DVD players, D-VHS, industrial cameras</td>
</tr>
<tr>
<td>Other</td>
<td>Electronic instruments, electric bidets, toys, learning devices, remote controllers, etc.</td>
</tr>
</tbody>
</table>
5 Keys of V850

High performance
Performance ranging from 20 to over 300 MIPS with single instruction set

- Compared to 8-/16-bit microcontroller, offer a MIPS performance 10 or more times higher for the same frequency, and 2 to 3 times higher at the actual application level (based on NEC evaluation)
- System operation at frequencies 1/2 to 1/3 those of 8-/16-bit microcontrollers is enabled, contributing to lowering system power consumption.
- The V850 core, V850ES core, V850E1 core, and V850E2 core are upward compatible at the object level.

Additional functions
Realization of systems with high added value through the addition of supplementary functions to existing systems via middleware
Realization of functions heretofore realized with peripheral ICs through V850 + middleware, reducing development time and reducing system costs
Rich lineup of video, audio, network-related, and other middleware tuned for V850 Series

Product lineup
Low-end/Middle-range/High-end/ASSP deployment

- Low-end lineup: Kx1 Series of general-purpose microcontrollers for 16 to 32-bit market designed for high cost-performance.
- Middle-range lineup: Low noise, low power consumption, large-capacity memory lineup, low-voltage operation support
- High-End lineup: Designed for high performance, on-chip memory controller and DMA
- ASSP lineup: Field-specific product lineup, on-chip dedicated hardware

Images and diagrams illustrating product lineup and additional functions.

Roadmap/Features
5 points supporting the high performance of the V850 Series

- High performance
- Product lineup
- Additional functions
The V850 Series is also being actively expanded for ASIC CPU cores, realizing smooth transition to system LSIs. The following elements essential for system LSIs are provided on a timely basis:

1. Leading-edge process technology
2. High-performance CPU core
3. Rich lineup of IP cores
4. Top-down design environment
5. Flexible application design

- Micro-fabrication technology
- Multi-layer wiring technology
- Mixed-process technology
- High-pin-count packages
- MPU, DSP, DRAM, SRAM, AV, communication, BUS, high-speed I/O

Voice recognition/synthesis
AV processing
(JPEG1, MPEG1, etc.)
Modem

PM development environment
Utilization of existing functions
Improved usability

PM Project Manager
78K development environment
GC (Compiler)
RX (Real-time OS)
SM (Simulator)
ID (Debugger)
IE, IECUBE (In-circuit emulator)

V850 development environment
CA (Compiler)
RX (Real-time OS)
LRD (task debugger)
SA2 (analysior)
SM (Simulator)
ID (Debugger)
IE, IECUBE (In-circuit emulator)

V850 products
Realization of high-performance powerful development environment making use of
- High performance
- General-purpose
- Large memory capacity

IECUBE™, a low-cost high-performance emulator, and N-Wire CARD, an ultra-low cost on-chip emulator are available.

- Realization of better connectivity with target boards, addition of GUI customization function, improved online help, etc.
- Realization of shorter development TAT through support of quick and accurate software development via a rich development environment lineup featuring easy operation and sophisticated functions.

- Design environment
  - Chip design environment
  - Synthesis/verification
  - Software development environment
  - Hardware/software-coordinated design

- Middleware
  - Voice recognition/synthesis
  - AV processing
  - (JPEG1, MPEG1, etc.)

- Chip design environment
  - Synthesis/verification
  - Software development environment
  - Hardware/software-coordinated design

- System LSI
  - Smooth transition to system LSIs
**Product Lineup**

### Kx1 Series lineup

**Rich memory & package lineup**

<table>
<thead>
<tr>
<th>ROM (Bytes)</th>
<th>296K</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V850ES</strong></td>
<td></td>
</tr>
<tr>
<td>128K</td>
<td></td>
</tr>
<tr>
<td>96K</td>
<td></td>
</tr>
<tr>
<td>64K</td>
<td></td>
</tr>
<tr>
<td>32K</td>
<td></td>
</tr>
<tr>
<td>16K</td>
<td></td>
</tr>
<tr>
<td>8K</td>
<td></td>
</tr>
<tr>
<td>4K</td>
<td></td>
</tr>
<tr>
<td>2K</td>
<td></td>
</tr>
<tr>
<td>1K</td>
<td></td>
</tr>
</tbody>
</table>

**Low-End Lineup**

**78K0/Kxx**

- **V850ES/KF1**
  - 80-pin version
  - Single-power-supply flash
  - On-chip POC/LVI
  - On-chip debugging function
  - DMA function (only KG1+, KJ1+)

- **V850ES/KG1**
  - 100-pin version
  - 144-pin version

- **V850ES/KJ1**
  - 100-pin version
  - 144-pin version

**V850ES/KE1**

- 64-pin version
- 80-pin version
- 100-pin version

**V850ES/KF1**

- 64-pin version
- 80-pin version

**V850ES/KG1**

- 100-pin version

**V850ES/KJ1**

- 144-pin version

### Kx1 Series lineup

**Seamless lineup**

<table>
<thead>
<tr>
<th>ROM (Bytes)</th>
<th>296K</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V850ES</strong></td>
<td></td>
</tr>
<tr>
<td>128K</td>
<td></td>
</tr>
<tr>
<td>96K</td>
<td></td>
</tr>
<tr>
<td>64K</td>
<td></td>
</tr>
<tr>
<td>32K</td>
<td></td>
</tr>
<tr>
<td>16K</td>
<td></td>
</tr>
<tr>
<td>8K</td>
<td></td>
</tr>
<tr>
<td>4K</td>
<td></td>
</tr>
<tr>
<td>2K</td>
<td></td>
</tr>
<tr>
<td>1K</td>
<td></td>
</tr>
</tbody>
</table>

**Low EMI noise design**

**Development environment usable in common for all series**

**Wide voltage range support (2.7 to 5.5 V)**

**Single-power-supply flash lineup**

(self programming, EEPROM™ emulation support)

### Kx1+ features

**Kx1+ are microcontrollers featuring additional functions.**

- **Runaway detection function**
  - Watchdog timer running on main clock

- **Voltage detection circuit**
  - None

- **Reset functions**
  - External reset, WDT reset

- **DMA function**
  - None

- **Oscillation stabilization time reduction**
  - Fixed at reset release

- **A/D converter**
  - Conversion time 14 µs (min.)
  - Successive approximation mode

- **LIN bus interface**
  - No hardware

### Product specifications

**Item** | KE1 | KF1 | KG1 | KJ1 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
</tr>
<tr>
<td>Performance</td>
<td>24 MHz (at 20 MHz)</td>
<td>20 MHz (main clock)</td>
<td>20 MHz (main clock)</td>
<td>20 MHz (main clock)</td>
</tr>
<tr>
<td>Maximum operating frequency</td>
<td>32.768 kHz (subclock)</td>
<td>32.768 kHz (subclock)</td>
<td>32.768 kHz (subclock)</td>
<td>32.768 kHz (subclock)</td>
</tr>
<tr>
<td>Strobe flash memory</td>
<td>128 KB</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
</tr>
<tr>
<td>External flash memory</td>
<td>16 KB</td>
<td>128 KB</td>
<td>128 KB</td>
<td>128 KB</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB</td>
<td>128 KB/256 KB/4 KB</td>
<td>128 KB/256 KB/4 KB</td>
<td>128 KB/256 KB/4 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>4.0 V to 5.5 V @ 20 MHz</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>150 mW (20 MHz @ 5V)</td>
<td>150 mW (20 MHz @ 5V)</td>
<td>150 mW (20 MHz @ 5V)</td>
<td>150 mW (20 MHz @ 5V)</td>
</tr>
<tr>
<td>External bus</td>
<td>-</td>
<td>Address: Multiplexed</td>
<td>Address: Multiplexed/separate</td>
<td>Address: Multiplexed/separate</td>
</tr>
<tr>
<td>Timer/clock</td>
<td>16-bit 2 ch</td>
<td>16-bit 2 ch (256 KB)</td>
<td>16-bit 4 ch (256 KB)</td>
<td>16-bit 4 ch (256 KB)</td>
</tr>
<tr>
<td></td>
<td>3 ch</td>
<td>3 ch</td>
<td>3 ch</td>
<td>3 ch</td>
</tr>
<tr>
<td></td>
<td>Data: 8/16-bit</td>
<td>Data: 8/16-bit</td>
<td>Data: 8/16-bit</td>
<td>Data: 8/16-bit</td>
</tr>
<tr>
<td></td>
<td>Watch transfer ch</td>
<td>Watch transfer ch</td>
<td>Watch transfer ch</td>
<td>Watch transfer ch</td>
</tr>
<tr>
<td>Analog interface</td>
<td>CS1n2 ch, UART1-2 ch</td>
<td>CS1n4 ch, UART1-2 ch</td>
<td>CS1n2 ch, UART1-2 ch</td>
<td>CS1n2 ch, UART1-2 ch</td>
</tr>
<tr>
<td></td>
<td>1C1x1 ch</td>
<td>1C1x1 ch</td>
<td>1C1x1 ch</td>
<td>1C1x1 ch</td>
</tr>
<tr>
<td></td>
<td>CS1 with automatic transfer function1 ch</td>
<td>CS1 with automatic transfer function2 ch</td>
<td>CS1 with automatic transfer function1 ch</td>
<td>CS1 with automatic transfer function2 ch</td>
</tr>
<tr>
<td></td>
<td>CS2n2 ch, UART1-2 ch</td>
<td>CS2n2 ch, UART1-2 ch</td>
<td>CS2n2 ch, UART1-2 ch</td>
<td>CS2n2 ch, UART1-2 ch</td>
</tr>
<tr>
<td></td>
<td>1C1x1 ch</td>
<td>1C1x1 ch</td>
<td>1C1x1 ch</td>
<td>1C1x1 ch</td>
</tr>
<tr>
<td></td>
<td>CS1 with automatic transfer function1 ch</td>
<td>CS1 with automatic transfer function2 ch</td>
<td>CS1 with automatic transfer function1 ch</td>
<td>CS1 with automatic transfer function2 ch</td>
</tr>
<tr>
<td>Power consumption</td>
<td>10 mW @ 4 MHz (5V)</td>
<td>10 mW @ 4 MHz (5V)</td>
<td>10 mW @ 4 MHz (5V)</td>
<td>10 mW @ 4 MHz (5V)</td>
</tr>
<tr>
<td>Package</td>
<td>64-pin TQFP(12x12 mm)</td>
<td>64-pin TQFP(10x10 mm)</td>
<td>64-pin TQFP(14x14 mm)</td>
<td>64-pin TQFP(14x14 mm)</td>
</tr>
<tr>
<td></td>
<td>64-pin LQFP(12x12 mm)</td>
<td>64-pin LQFP(10x10 mm)</td>
<td>64-pin LQFP(14x14 mm)</td>
<td>64-pin LQFP(14x14 mm)</td>
</tr>
<tr>
<td></td>
<td>80-pin LLP(12x12 mm)</td>
<td>80-pin LLP(14x14 mm)</td>
<td>80-pin LLP(14x14 mm)</td>
<td>80-pin LLP(14x14 mm)</td>
</tr>
<tr>
<td></td>
<td>100-pin LLP(20x20 mm)</td>
<td>100-pin LLP(20x20 mm)</td>
<td>100-pin LLP(20x20 mm)</td>
<td>100-pin LLP(20x20 mm)</td>
</tr>
</tbody>
</table>

* Only Y products have an on-chip PC interface.
System cost reduction

**Conventional set**
- Voltage detector
- Voltage drop detection
- WDT independent from CPU clock

**Kx1 Series Not set**
- Peripheral functions on single chip
- System reset voltage detection

**Common peripheral functions**

Large array of peripheral functions common with 8-bit 78K0 Series

---

**Table: Comparison of Kx1 Series**

<table>
<thead>
<tr>
<th>Item</th>
<th>VE80/E/E1+</th>
<th>VE80S/E</th>
<th>VE80S/E1+</th>
<th>VE80S/E10+</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>VE80S VE80S</td>
<td>VE80S</td>
<td>VE80S</td>
<td>VE80S</td>
</tr>
<tr>
<td>Performance</td>
<td>20 MHz (20 MHz)</td>
<td>20 MHz (20 MHz)</td>
<td>20 MHz (20 MHz)</td>
<td>20 MHz (20 MHz)</td>
</tr>
<tr>
<td>Maximum operating frequency</td>
<td>32.768 MHz (outlock)</td>
<td>32.768 MHz (outlock)</td>
<td>32.768 MHz (outlock)</td>
<td>32.768 MHz (outlock)</td>
</tr>
<tr>
<td>Internal flash memory</td>
<td>128 KB</td>
<td>128 KB</td>
<td>128 KB</td>
<td>128 KB</td>
</tr>
<tr>
<td>External flash memory</td>
<td>67 KB</td>
<td>67 KB</td>
<td>67 KB</td>
<td>67 KB</td>
</tr>
<tr>
<td>Clock Monitor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>4.5 V to 5.5 V @ 20 MHz</td>
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<td>4.5 V to 5.5 V @ 20 MHz</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
<td>4.0 V to 5.5 V @ 16 MHz</td>
</tr>
<tr>
<td>Timer/counter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>External bus</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-chip reset function</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal interface</td>
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</tr>
<tr>
<td>Analog comparator</td>
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<tr>
<td>On-chip debug function</td>
<td></td>
<td></td>
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<tr>
<td>I/O</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>ROM correction function, real-time output, key return function</td>
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</tr>
<tr>
<td>I2C</td>
<td></td>
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<tr>
<td>UART</td>
<td></td>
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</tr>
<tr>
<td>Timer</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Port</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

---

* Only V products have an on-chip I2C interface.
**Product Lineup**

**Middle-Range Lineup**

Large-capacity memory, 2.5 V/3 V/5 V general-purpose product lineup

- **V850/SC1**
  - 5 V low-power version
  - 144-pin version
  - 5 V I²C interface

- **V850/SB1**
  - 5 V low-power version
  - 100-pin version

- **µPD703229Y**
  - 5 V large-capacity RAM version
  - 100-pin version

- **V850ES/SJx**
  - Single-power-supply flash
  - Larger capacity memory
  - Enhanced peripheral functions

- **V850ES/SJ2**
  - Single-power-supply flash
  - Larger capacity memory
  - High-capacity RAM

- **V850ES/ST2**
  - Low voltage, super-low power consumption

- **V850ES/SA2**
  - Low voltage, super-low power consumption

- **V850ES/SA3**
  - Low power, super-low power consumption

---

**Product specifications**

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/Sx2</th>
<th>V850ES/Sx3</th>
<th>µPD703229Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU clock</td>
<td>20 MHz (20 MHz)</td>
<td>20 MHz (20 MHz)</td>
<td>20 MHz (20 MHz)</td>
</tr>
<tr>
<td>Maximum operating frequency</td>
<td>32.768 kHz (subclock)</td>
<td>32.768 kHz (subclock)</td>
<td>32.768 kHz (subclock)</td>
</tr>
<tr>
<td>Flash memory</td>
<td>256 KB</td>
<td>256 KB</td>
<td>512 KB</td>
</tr>
<tr>
<td>External flash ROM</td>
<td>256 KB</td>
<td>256 KB</td>
<td>512 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>1.8 V to 2.7 V</td>
<td>2.5 V to 3.3 V</td>
<td>3.0 V to 5.5 V</td>
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<tr>
<td>Power supply voltage</td>
<td>1.8 V to 2.7 V</td>
<td>2.5 V to 3.3 V</td>
<td>3.0 V to 5.5 V</td>
</tr>
<tr>
<td>Address: Multiplexed/separate</td>
<td>V850ES/Sx2</td>
<td>V850ES/Sx3</td>
<td>µPD703229Y</td>
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<tr>
<td>Processor</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td>RAM controller</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td>I/O function</td>
<td>1 ch</td>
<td>1 ch</td>
<td>1 ch</td>
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<tr>
<td>Peripheral function</td>
<td>TDC</td>
<td>TDC</td>
<td>TDC</td>
</tr>
<tr>
<td>Power consumption</td>
<td>38 mW</td>
<td>54 mW</td>
<td>50 mW</td>
</tr>
</tbody>
</table>

- Note: Products without automotive bus, products with on-chip I²C bus, and products with on-chip aFCAN are available.

---

**Large-capacity memory, 2.5 V/3 V/5 V general-purpose product lineup**

- **V850/SA1**
  - 3 V low-power version

- **V850ES/Sx3**
  - Single-power-supply flash
  - Larger capacity memory
  - Enhanced peripheral functions

- **V850ES/SA2**
  - Low voltage, super-low power consumption

- **V850ES/SA3**
  - Low power, super-low power consumption

---

**Middle-Range Lineup**

- **V850/SC1**
  - 5 V low-power version
  - 144-pin version
  - 5 V I²C interface

- **V850/SB1**
  - 5 V low-power version
  - 100-pin version

- **µPD703229Y**
  - 5 V large-capacity RAM version
  - 100-pin version

- **V850ES/SJx**
  - Single-power-supply flash
  - Larger capacity memory
  - Enhanced peripheral functions

- **V850ES/SJ2**
  - Single-power-supply flash
  - Larger capacity memory
  - High-capacity RAM

- **V850ES/ST2**
  - Low voltage, super-low power consumption

- **V850ES/SA2**
  - Low voltage, super-low power consumption

- **V850ES/SA3**
  - Low power, super-low power consumption

---

**Under planning**

**Under development**

**In mass production**

**5 V general-purpose**

- **Low noise**

**3 V general-purpose**

- **Low power consumption**

---

**Note**

- Products without automotive bus, products with on-chip I²C bus, and products with on-chip aFCAN are available.
### V850ES/SG2, SJ2
- Low EMI noise
- 20 MHz @ 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM: 256 KB/48 KB, 512 KB/40 KB, 384 KB/32 KB, 256 KB/24 KB (SG2 only)
- Automotive on-chip bus support: IEBus*, aFCAN* (*: Only products with on-chip SG2, SJ2)
- On-chip debugging function
- 100-pin QFP (SG2)/100-pin LQFP (SG2)/144-pin LQFP (SJ2)

### V850ES/SA2, SA3
- Min. 2.2 V low-voltage operation (including A/D, D/A converter, flash)
- Low power consumption and high-speed operation during 38 mW @ 2.5 V, 20 MHz operation
- Single-power-supply flash
- ROM/RAM: 512 KB/24 KB, 384 KB/24 KB, 256 KB/16 KB, 128 K/8 KB
- Thin and compact package support: 100-pin TQFP/121-pin FBGA (SA3)

### V850/SB1
- Low EMI noise
- Large-capacity memory and large memory selection
- ROM/RAM: 512 KB/24 KB, 384 KB/24 KB, 256 KB/16 KB, 128 K/8 KB
- 100-pin QFP/100-pin LQFP

### V850/SC1
- Low EMI noise
- Large-capacity memory (ROM/RAM: 512 KB/24 KB)
- Enhanced peripheral functions for SB1
- 144-pin LQFP

---

<table>
<thead>
<tr>
<th>Feature</th>
<th>V850ES/SG2, SJ2</th>
<th>V850ES/SA2, SA3</th>
<th>V850/SB1</th>
<th>V850/SC1</th>
<th>V850ES/ST2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
<td>V850ES</td>
</tr>
<tr>
<td>Performance</td>
<td>25 MIPs (20 MHz)</td>
<td>25 MIPs (20 MHz)</td>
<td>23 MIPs (20 MHz)</td>
<td>23 MIPs (20 MHz)</td>
<td>23 MIPs (34 MHz)</td>
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<tr>
<td>Maximum operating frequency</td>
<td>32,768 kHz (subclock)</td>
<td>32,768 kHz (subclock)</td>
<td>32,768 kHz (subclock)</td>
<td>32,768 kHz (subclock)</td>
<td>32,768 kHz (subclock)</td>
</tr>
<tr>
<td>Internal flash memory</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
<td>256 KB/128 KB</td>
</tr>
<tr>
<td>External flash ROM</td>
<td>512 KB/256 KB/128 KB</td>
<td>512 KB/256 KB/128 KB</td>
<td>512 KB/256 KB/128 KB</td>
<td>512 KB/256 KB/128 KB</td>
<td>512 KB/256 KB/128 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.0 V to 5.5 V (flash memory versions)</td>
<td>3.0 V to 5.5 V (flash memory versions)</td>
<td>3.0 V to 5.5 V (flash memory versions)</td>
<td>3.0 V to 5.5 V (flash memory versions)</td>
<td>3.0 V to 5.5 V (flash memory versions)</td>
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<td>Power supply voltage</td>
<td>3.3 V to 5.5 V (mean ROM version)</td>
<td>3.3 V to 5.5 V (mean ROM version)</td>
<td>3.3 V to 5.5 V (mean ROM version)</td>
<td>3.3 V to 5.5 V (mean ROM version)</td>
<td>3.3 V to 5.5 V (mean ROM version)</td>
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<tr>
<td>External bus</td>
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<td>Multiplexed/separate</td>
<td>Multiplexed/separate</td>
<td>Multiplexed/separate</td>
<td>Multiplexed/separate</td>
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<tr>
<td>Data: 16-bit</td>
<td>8-bit-4 ch, 8-bit-6 ch, 8-bit-8 ch</td>
<td>8-bit-4 ch, 8-bit-6 ch, 8-bit-8 ch</td>
<td>8-bit-4 ch, 8-bit-6 ch, 8-bit-8 ch</td>
<td>8-bit-4 ch, 8-bit-6 ch, 8-bit-8 ch</td>
<td>8-bit-4 ch, 8-bit-6 ch, 8-bit-8 ch</td>
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<tr>
<td>Timers/counter</td>
<td>Watch timer-1 ch</td>
<td>Watch timer-1 ch</td>
<td>Watch timer-1 ch</td>
<td>Watch timer-1 ch</td>
<td>Watch timer-1 ch</td>
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<td>CS1-1 ch, CS1 UAR1-2 ch, CS1 UAR1-2 ch</td>
<td>CS1-1 ch, CS1 UAR1-2 ch, CS1 UAR1-2 ch</td>
<td>CS1-1 ch, CS1 UAR1-2 ch, CS1 UAR1-2 ch</td>
<td>CS1-1 ch, CS1 UAR1-2 ch, CS1 UAR1-2 ch</td>
<td>CS1-1 ch, CS1 UAR1-2 ch, CS1 UAR1-2 ch</td>
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<tr>
<td>DMA controller</td>
<td>16-bit-1 ch, 16-bit-2 ch</td>
<td>16-bit-1 ch, 16-bit-2 ch</td>
<td>16-bit-1 ch, 16-bit-2 ch</td>
<td>16-bit-1 ch, 16-bit-2 ch</td>
<td>16-bit-1 ch, 16-bit-2 ch</td>
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<tr>
<td>DMA converter</td>
<td>16-bit-12 ch</td>
<td>16-bit-12 ch</td>
<td>16-bit-12 ch</td>
<td>16-bit-12 ch</td>
<td>16-bit-12 ch</td>
</tr>
<tr>
<td>DMA controller (internal extension)</td>
<td>6-channel (6-ch internal RAM-on-chip peripheral (L))</td>
<td>6-channel (6-ch internal RAM-on-chip peripheral (L))</td>
<td>6-channel (6-ch internal RAM-on-chip peripheral (L))</td>
<td>6-channel (6-ch internal RAM-on-chip peripheral (L))</td>
<td>6-channel (6-ch internal RAM-on-chip peripheral (L))</td>
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<tr>
<td>DMA controller (external extension)</td>
<td>6-channel (6-ch external RAM-on-chip peripheral (D))</td>
<td>6-channel (6-ch external RAM-on-chip peripheral (D))</td>
<td>6-channel (6-ch external RAM-on-chip peripheral (D))</td>
<td>6-channel (6-ch external RAM-on-chip peripheral (D))</td>
<td>6-channel (6-ch external RAM-on-chip peripheral (D))</td>
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<tr>
<td>Power consumption</td>
<td>66 mW (10 MHz @ 3.3 V)</td>
<td>66 mW (17 MHz @ 5 V)</td>
<td>125 mW (20 MHz @ 5 V)</td>
<td>125 mW (20 MHz @ 5 V)</td>
<td>125 mW (20 MHz @ 5 V)</td>
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<tr>
<td>Package</td>
<td>100-pin LQFP (14x14 mm)</td>
<td>100-pin LQFP (14x14 mm)</td>
<td>100-pin LQFP (14x14 mm)</td>
<td>100-pin LQFP (14x14 mm)</td>
<td>100-pin LQFP (14x14 mm)</td>
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<td>Base pin</td>
<td>85</td>
<td>85</td>
<td>124</td>
<td>65</td>
<td>65</td>
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</tbody>
</table>

*Only Y products have an on-chip FC interface.

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**V850/SA1**
- Low power consumption and high-speed operation during 66 mW @ 3.3 V, 20 MHz operation
- Large memory selection
- ROM/RAM: 256 KB/8 KB, 128 KB/4 KB, 64 KB/4 KB
- 100-pin LQFP/121-pin FBGA

**V850/SC1**
- Low power consumption and high-speed operation during 66 mW @ 3.3 V, 20 MHz operation
- Large memory selection
- ROM/RAM: 256 KB/8 KB, 128 KB/4 KB, 64 KB/4 KB
- 100-pin LQFP/121-pin FBGA

**V850/ST2**
- ROM-less version
- On-chip high-capacity RAM (48 KB)
- 3.3 V, 34 MHz operation
- Thin-type, compact type packages supported: 120-pin TQFP/144-pin LQFP
## Features

**V850E/ME2**
- 215 MIPS @150 MHz, internal 1.5 V/external 3.3 V operation ROM-less microcontroller
- Large-capacity internal RAM (128 KB), real-time control
- On-chip SSCG*, EMI peak reduction
- USB full-speed (function), on-chip debugging function
- On-chip SDRAM interface
- 176-pin LGFP/240-pin FBGA

*Spread Spectrum Frequency Synthesizer Clock Generator

**V850E/MA1,MA2**
- 67 MIPS @50 MHz
- Internal 3.3 V/external 5 V tolerant operation single-chip microcontroller (MA1)
- ROM-less product lineup also available
- 40 MHz @3.3 V ROM-less microcontroller (MA2)
- ROM/RAM: 256 KB/10 KB (MA1), ROM-less/4 KB (MA1, MA2)
- On-chip SDRAM interface, DMA
- 144-pin LGFP/161-pin FBGA (MA1), 100-pin LGFP (MA2)

**V850E/MA3**
- 106 MIPS @80 MHz, internal 2.5 V/external 3.3 V operation single-chip microcontroller
- Large-capacity internal ROM/RAM (512 KB/32 KB)
- Internal single power supply flash
- SDRAM interface, motor control function, on-chip debugging function
- 144-pin LGFP/161-pin FBGA

**V850E/MS1,MS2**
- 47 MIPS @33 MHz, 3.3 V & 5 V single-chip microcontroller (MS1)
- ROM-less product (Max. 40 MHz) lineup available
- 39 MHz @ internal 3.3 V/external 5 V ROM-microcontroller (MS2)
- ROM/RAM: 128 KB/4 KB (MS1), ROM-less/4 KB (MS1, MS2)
- 144-pin LGFP (MS1)/157-pin FBGA (MS1)/100-pin LGFP (MS2)

## Product specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/ME2</th>
<th>V850E/MA1</th>
<th>V850E/MA2</th>
<th>V850E/MA3</th>
<th>V850E/MS1</th>
<th>V850E/MS2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td>2.0 W (40 MHz)</td>
<td>1.5 W</td>
<td>2.0 W (40 MHz)</td>
<td>2.0 W (40 MHz)</td>
<td>1.5 W</td>
<td>2.0 W (40 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>144-pin LGFP</td>
<td>144-pin LGFP</td>
<td>144-pin LGFP</td>
<td>144-pin LGFP</td>
<td>144-pin LGFP</td>
<td>144-pin LGFP</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
<td>3.0 V to 3.6 V (external)</td>
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<tr>
<td>Memory controller</td>
<td>SRAM, DRAM, etc.</td>
<td>SRAM, DRAM, etc.</td>
<td>SRAM, DRAM, etc.</td>
<td>SRAM, DRAM, etc.</td>
<td>SRAM, DRAM, etc.</td>
<td>SRAM, DRAM, etc.</td>
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<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
<td>Address: Separate</td>
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<td>Timematcher</td>
<td>16-bit/12-bit</td>
<td>16-bit/12-bit</td>
<td>16-bit/12-bit</td>
<td>16-bit/12-bit</td>
<td>16-bit/12-bit</td>
<td>16-bit/12-bit</td>
</tr>
<tr>
<td>DMA controller</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
</tr>
<tr>
<td>I/O port</td>
<td>100-pin</td>
<td>100-pin</td>
<td>100-pin</td>
<td>100-pin</td>
<td>100-pin</td>
<td>100-pin</td>
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<td>Power consumption (typ.)</td>
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<td>300 mW (50 MHz @ 1.5 V)</td>
<td>300 mW (50 MHz @ 1.5 V)</td>
<td>300 mW (50 MHz @ 1.5 V)</td>
<td>300 mW (50 MHz @ 1.5 V)</td>
<td>300 mW (50 MHz @ 1.5 V)</td>
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</table>

Note: 1.35 V to 1.65 V @ 10 MHz to 133 MHz
1.40 V to 1.65 V @ 10 MHz to 150 MHz
Application examples

MFP (Multifunction printer)

Thermal printer

DVD player

Fax machine
## Product Lineup

### ASSP Lineup (1)

#### Field-specific lineups

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<tr>
<th>Product</th>
<th>V850E/IA1</th>
<th>V850E/IA2</th>
<th>V850E/IA3</th>
<th>V850E/IA4</th>
<th>V850ES/K1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Features</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For inverter control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For camcorders (incl. DVC)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For power meter control</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

#### V850E/IA3, IA4

- **For inverter control**
  - 82 MIPS @ 64 MHz, internal 2.5 V/external 5 V operation
  - On-chip 6-phase sinusoidal PWM timer, on-chip operational amplifier/comparator, on-chip high-speed A/D
  - On-chip debugging function (IA4 only)
  - ROM/RAM: 256 KB/12 KB, 128 KB/6 KB (mask ROM version only)
  - 80-pin QFP (IA3), 100-pin LQFP/100-pin QFP (IA4)

#### V850ES/K1

- **For inverter control**
  - 41 MIPS @ 32 MHz, 4.5 V to 5.5 V (on-chip regulator)
  - On-chip 6-phase sinusoidal PWM timer, POC/LVI, and clock monitor functions
  - ROM/RAM: 128 KB/6 KB, 64 KB/4 KB
  - 64-pin LQFP

### Features

- **V850E/IA3, IA4**
  - For inverter control
  - 82 MIPS @ 64 MHz, internal 2.5 V/external 5 V operation
  - On-chip 6-phase sinusoidal PWM timer, on-chip operational amplifier/comparator, on-chip high-speed A/D
  - On-chip debugging function (IA4 only)
  - ROM/RAM: 256 KB/12 KB, 128 KB/6 KB (mask ROM version only)
  - 80-pin QFP (IA3), 100-pin LQFP/100-pin QFP (IA4)

- **V850ES/K1**
  - For inverter control
  - 41 MIPS @ 32 MHz, 4.5 V to 5.5 V (on-chip regulator)
  - On-chip 6-phase sinusoidal PWM timer, POC/LVI, and clock monitor functions
  - ROM/RAM: 128 KB/6 KB, 64 KB/4 KB
  - 64-pin LQFP

### Product specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>V850E/IA1</th>
<th>V850E/IA2</th>
<th>V850E/IA3</th>
<th>V850E/IA4</th>
<th>V850ES/K1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Performance</td>
<td>67 MIPS @ 10 MHz</td>
<td>64 MIPS @ 40 MHz</td>
<td>64 MIPS @ 40 MHz</td>
<td>64 MIPS @ 40 MHz</td>
<td>41 MIPS @ 32 MHz</td>
</tr>
<tr>
<td>Internal single-power supply</td>
<td>60 MHz</td>
<td>40 MHz</td>
<td>64 MHz</td>
<td>64 MHz</td>
<td>64 MHz</td>
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<tr>
<td>Internal mask ROM</td>
<td>256 KF</td>
<td>128 KF</td>
<td>128 KF</td>
<td>128 KF</td>
<td>256 KF</td>
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<tr>
<td>Power supply voltage</td>
<td>3.5 V to 5.5 V (internal)</td>
<td>4.5 V to 5.5 V (external)</td>
<td>3.5 V to 2.7 V (internal)</td>
<td>4.5 V to 5.5 V (external)</td>
<td>3.5 V to 2.7 V (internal)</td>
</tr>
<tr>
<td>External bus</td>
<td>Address/Multiplexed Data: 8/16 bits</td>
<td>Address/Multiplexed Data: 8/16 bits</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Timer counter</td>
<td>16bit x 8 ch</td>
<td>16bit x 7 ch</td>
<td>16bit x 4 ch</td>
<td>16bit x 4 ch</td>
<td>16bit x 4 ch</td>
</tr>
<tr>
<td>Serial interface</td>
<td>CSI = 3ch, UART = 3ch</td>
<td>CSI = 1 ch, CSI/UART = 1 ch</td>
<td>CSI = 1 ch, CSI/UART = 1 ch</td>
<td>CSI = 1 ch, CSI/UART = 1 ch</td>
<td>CSI = 1 ch, UART = 2 ch</td>
</tr>
<tr>
<td>ADC converter</td>
<td>10bit x (8 ch + 8 ch)</td>
<td>10bit x (4 ch + 2 ch)</td>
<td>10bit x (4 ch + 2 ch)</td>
<td>10bit x (4 ch + 2 ch)</td>
<td>10bit x (4 ch + 2 ch)</td>
</tr>
<tr>
<td>SPI converter</td>
<td>4 ch</td>
<td>4 ch</td>
<td>-</td>
<td>-</td>
<td>4 ch</td>
</tr>
<tr>
<td>Serial peripheral functions</td>
<td>FUD/UART = 2 ch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.8 W</td>
<td>1.5 W</td>
<td>1.75 W</td>
<td>1.75 W</td>
<td>1.8 W</td>
</tr>
<tr>
<td>Package</td>
<td>144-pin LQFP (20 x 20 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>80-pin QFP (14 x 14 mm)</td>
<td>100-pin QFP (14 x 10 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
</tr>
</tbody>
</table>

### Inverter control

- On-chip inverter and timer

### DVC control

- On-chip VCR servo timer

### Power meter instrument measuring control

- On-chip 16-bit ΔΣADC

---

Pamphlet U15412EJ4V1PF

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### Application examples

#### Air conditioner

**V850E/IA4**

- **Compressor motor**
- **Outdoor unit**
- **Indoor unit**

#### Digital Video Camera

**V850E/SV2**

- **Camera control block**
- **Display controller**
- **System control & servo control block**

#### Power meter

**V850ES/PM1**

- **Main clock**
- **Subclock**

---

<table>
<thead>
<tr>
<th>Item</th>
<th>V850/SV1</th>
<th>V850E/SV2</th>
<th>V850ES/PM1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU performance</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>55 MIPS (@ 20.5 MHz)</td>
<td>29 MIPS (90 MHz)</td>
</tr>
<tr>
<td>Source words (n)</td>
<td>32-bit</td>
<td>32-bit</td>
<td>32-bit</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>256 KB</td>
<td>128 KB</td>
<td>10 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>5.0 V to 3.3 V (internal)</td>
<td>2.7 V to 3.6 V (external)</td>
<td>2.2 to 3.6 V @ 32.768 kHz</td>
</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit</td>
<td>16-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td>A/D converter</td>
<td>10-bit</td>
<td>10-bit</td>
<td>10-bit</td>
</tr>
<tr>
<td>DMA controller</td>
<td>8-bit</td>
<td>8-bit</td>
<td>8-bit</td>
</tr>
<tr>
<td>Power consumption</td>
<td>35.5 W (20 MHz)</td>
<td>40.0 W (20 MHz)</td>
<td>130 mW (20 MHz)</td>
</tr>
</tbody>
</table>

* Only Y products have an on-chip I²C interface.*
**ASSP Lineup (2)**

**V850/DB1**
- For automotive electronics (body control applications)
- ROM/RAM: 128 KB/6 KB
- On-chip DCAN controller (2 ch max.)
- 18 MIPS @ 16 MHz, 4.0 to 5.5 V operation
- 128-pin QFP

**V850ES/FE2, FF2, FG2, FJ2**
- For automotive electronics (body control applications)
- ROM/RAM: 512 KB/20 KB, 384 KB/16 KB, 256 KB/12 KB, 128 KB/6 KB
- On-chip aFCAN controller (4 ch max.), LIN function
- 29 MIPS @ 20 MHz, 4.0 to 5.5 V operation
- 64-pin TQFP (FE2)/80-pin TQFP (FF2)/100-pin LQFP (FG2)/144-pin LQFP (FJ2)

**V850ES/SF1**
- For car audio
- Low EMI noise
- On-chip FCAN controller (2 ch max.)
- ROM/RAM: 256 KB/16 KB, 128 KB/12 KB
- 100-pin LQFP/100-pin QFP

**V850ES/SJ2**
- For car audio
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM: 640 KB/48 KB, 512 KB/32 KB, 256 KB/12 KB, 128 KB/6 KB
- On-chip IEBus controller (1 ch), on-chip aFCAN controller (2 ch max.)
- 90 MIPS @ 20 MHz, 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip debugging function
- 100-pin LQFP/100-pin QFP (SG2), 144-pin LQFP (SJ2)

**V850ES/SJx, SJ2**
- For car audio
- On-chip large-capacity single-power-supply flash memory
- ROM/RAM: 640 KB/48 KB, 512 KB/32 KB, 256 KB/12 KB, 128 KB/6 KB
- On-chip FCAN controller (1 ch), on-chip aFCAN controller (2 ch max.)
- 90 MIPS @ 20 MHz, 2.85 to 3.6 V operation
- 5 V withstand voltage ports incorporated, and 5 V output is possible by setting the N-ch open-drain output
- On-chip debugging function
- 100-pin LQFP/100-pin QFP (SG2), 144-pin LQFP (SJ2)

**Product specifications**

<table>
<thead>
<tr>
<th>Item</th>
<th>FE2</th>
<th>FF2</th>
<th>FG2</th>
<th>FJ2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU clock</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Performance</td>
<td>29 MIPS at 20 MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Return operating frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal flash memory</td>
<td>128 KB/64 KB</td>
<td>256 KB/128 KB</td>
<td>384 KB/256 KB</td>
<td>384 KB/256 KB</td>
</tr>
<tr>
<td>Internal mask ROM</td>
<td>128 KB/64 KB</td>
<td>256 KB/128 KB</td>
<td>384 KB/256 KB</td>
<td>384 KB/256 KB</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB/2 KB</td>
<td>4 KB/8 KB</td>
<td>4 KB/8 KB</td>
<td>4 KB/8 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>External bus</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer counter</td>
<td>16 bit x 16 bit</td>
<td>16 bit x 16 bit</td>
<td>16 bit x 16 bit</td>
<td>16 bit x 16 bit</td>
</tr>
<tr>
<td>Serial interface</td>
<td>CS1 x 2 ch, LIN-compatible UART = 2 ch</td>
<td>CS1 x 2 ch, LIN-compatible UART = 2 ch</td>
<td>CS1 x 3 ch, LIN-compatible UART = 3 ch</td>
<td>CS1 x 3 ch, LIN-compatible UART = 3 ch</td>
</tr>
<tr>
<td>Counter</td>
<td>10 bit x 16 bit</td>
<td>10 bit x 16 bit</td>
<td>10 bit x 16 bit</td>
<td>10 bit x 16 bit</td>
</tr>
<tr>
<td>DMA controller</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watch controller</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No peripheral</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby mode</td>
<td>150 mA (20 MHz @ 5 V)</td>
<td>200 mA (20 MHz @ 5 V)</td>
<td>200 mA (20 MHz @ 5 V)</td>
<td>200 mA (20 MHz @ 5 V)</td>
</tr>
<tr>
<td>Package</td>
<td>64-pin TQFP (19 x 10 mm)</td>
<td>80-pin TQFP (12 x 12 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>144-pin LQFP (20 x 20 mm)</td>
</tr>
</tbody>
</table>

**Dashboard control**
- On-chip meter driver
- On-chip LCD driver

**Body control**
- On-chip CAN

**Car audio control**
- On-chip CAN/On-chip IEBus
- Low noise
### Application examples

#### Dashboard

**Dashboard**  
**V850ES/Fx2**

#### Car audio

**Car Audio**  
**V850/SF1**

---

<table>
<thead>
<tr>
<th>Item</th>
<th>V850/ES2B</th>
<th>V850/SC2</th>
<th>V850/SC3</th>
<th>V850/SF1</th>
<th>V850/DB1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU MALFUNCTION</td>
<td>23 MHz</td>
<td>21 MHz</td>
<td>16 MHz</td>
<td>19 MHz</td>
<td>18 MHz</td>
</tr>
<tr>
<td>Main internal memory</td>
<td>512 KB</td>
<td>512 KB</td>
<td>512 KB</td>
<td>256 KB</td>
<td>128 KB</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>4.0 V to 5.5 V</td>
<td>3.5 V to 5.5 V</td>
<td>3.5 V to 5.5 V</td>
<td>3.5 V to 5.5 V</td>
<td>4.0 V to 5.5 V</td>
</tr>
<tr>
<td>External bus Address</td>
<td>Multiplexed</td>
<td>separate</td>
<td>Multiplexed</td>
<td>separate</td>
<td>-</td>
</tr>
<tr>
<td>Power consumption (operating frequency)</td>
<td>68 mW</td>
<td>68 mW</td>
<td>68 mW</td>
<td>68 mW</td>
<td>68 mW</td>
</tr>
<tr>
<td>Power consumption (standby)</td>
<td>85 mW</td>
<td>85 mW</td>
<td>85 mW</td>
<td>85 mW</td>
<td>85 mW</td>
</tr>
<tr>
<td>Power consumption (shut down)</td>
<td>90 mW</td>
<td>90 mW</td>
<td>90 mW</td>
<td>90 mW</td>
<td>90 mW</td>
</tr>
<tr>
<td>Package</td>
<td>128-pin QFP</td>
<td>128-pin LQFP</td>
<td>128-pin LQFP</td>
<td>128-pin LQFP</td>
<td>128-pin LQFP</td>
</tr>
</tbody>
</table>

---

- **V850/ES2B**
  - Low EMI noise
  - Large-capacity memory and large memory selection
  - ROM/RAM: 512K/24KB, 384KB/24KB, 256KB/16KB, 128KB/8KB
  - On-chip IEBus controller (1 ch)
  - 100-pin QFP/100-pin LQFP

- **V850/ES/Fx2**
  - Low EMI noise
  - Enhanced peripheral functions for SB1
  - On-chip IEBus controller (V850/SC2: 1 ch), On-chip FCAN controller (V850/SC3: 2 ch max.)
  - 144-pin LQFP

- **V850/SF1**
  - Low EMI noise
  - Enhanced-capacity memory (ROM/RAM: 512 KB/24 KB)
  - Enhanced peripheral functions for SB1
  - On-chip IEBus controller (V850/SC2: 1 ch)
  - 100-pin QFP/100-pin LQFP
# Product Lineup

## Memory Lineup

<table>
<thead>
<tr>
<th>ROM Size (bytes)</th>
<th>4K</th>
<th>6K</th>
<th>8K</th>
<th>10K</th>
<th>12K</th>
<th>16K</th>
<th>20K</th>
<th>24K</th>
<th>32K</th>
<th>40K</th>
<th>48K</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM Size (bytes)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ROM Size (bytes)</th>
<th>4K</th>
<th>6K</th>
<th>8K</th>
<th>10K</th>
<th>12K</th>
<th>16K</th>
<th>20K</th>
<th>24K</th>
<th>32K</th>
<th>40K</th>
<th>48K</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM Size (bytes)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Flash memory version

- MA1
- MA3
- SV1
- SJ2
- SG2

### Mask ROM version

- MS1
- KG1
- SF1

### Mask ROM/flash memory version

- MA3
- MA2
- SF1

* : Under development
## Package Lineup

<table>
<thead>
<tr>
<th>No. of pins</th>
<th>Type</th>
<th>Size</th>
<th>Pitch</th>
<th>Thickness</th>
<th>Mounted products</th>
</tr>
</thead>
<tbody>
<tr>
<td>121 pins</td>
<td>FBGA (F1)</td>
<td>12 x 12 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>SA1, SA3</td>
</tr>
<tr>
<td>161 pins</td>
<td>FBGA (F1)</td>
<td>13 x 13 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>MA1, MA3</td>
</tr>
<tr>
<td>180 pins</td>
<td>FBGA (F1)</td>
<td>14 x 14 mm</td>
<td>0.8 mm</td>
<td>0.96 mm</td>
<td>SV1</td>
</tr>
<tr>
<td>157 pins</td>
<td>FBGA (F1)</td>
<td>14 x 14 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>MS1</td>
</tr>
<tr>
<td>257 pins</td>
<td>FBGA (F1)</td>
<td>14 x 14 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>SV2</td>
</tr>
<tr>
<td>240 pins</td>
<td>FBGA (F1)</td>
<td>16 x 16 mm</td>
<td>0.8 mm</td>
<td>1.13 mm</td>
<td>ME2</td>
</tr>
<tr>
<td>64 pins</td>
<td>LQFP (GB)</td>
<td>10 x 10 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>KE1, KE1+</td>
</tr>
<tr>
<td>64 pins</td>
<td>TQFP (GB)</td>
<td>12 x 12 mm</td>
<td>0.5 mm</td>
<td>1.0 mm</td>
<td>FF2</td>
</tr>
<tr>
<td>64 pins</td>
<td>LQFP (GB)</td>
<td>14 x 14 mm</td>
<td>0.8 mm</td>
<td>1.4 mm</td>
<td>K1</td>
</tr>
<tr>
<td>80 pins</td>
<td>TQFP (GK)</td>
<td>12 x 12 mm</td>
<td>0.65 mm</td>
<td>1.0 mm</td>
<td>KF1, KF1+, FF2</td>
</tr>
<tr>
<td>80 pins</td>
<td>QFP (GF)</td>
<td>14 x 14 mm</td>
<td>0.8 mm</td>
<td>1.4 mm</td>
<td>K1</td>
</tr>
<tr>
<td>80 pins</td>
<td>QFP (GC)</td>
<td>14 x 14 mm</td>
<td>0.65 mm</td>
<td>1.4 mm</td>
<td>KF1, KF1+, IA3</td>
</tr>
<tr>
<td>100 pins</td>
<td>TQFP (GC)</td>
<td>14 x 14 mm</td>
<td>0.5 mm</td>
<td>1.0 mm</td>
<td>SN2</td>
</tr>
<tr>
<td>100 pins</td>
<td>TQFP (GC)</td>
<td>14 x 20 mm</td>
<td>0.65 mm</td>
<td>1.4 mm</td>
<td>SB1</td>
</tr>
<tr>
<td>120 pins</td>
<td>TQFP (GC)</td>
<td>14 x 14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>DB1</td>
</tr>
<tr>
<td>128 pins</td>
<td>LQFP (GJ)</td>
<td>14 x 14 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>J1, J1+, SC1, SC2, SC3, SJ2, ST2, FJ2, MS1, MA1, MA3, IA1</td>
</tr>
<tr>
<td>176 pins</td>
<td>LQFP (GM)</td>
<td>24 x 24 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>SV1, ME2</td>
</tr>
<tr>
<td>128 pins</td>
<td>QFP (GJ)</td>
<td>20 x 20 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>SA2</td>
</tr>
<tr>
<td>144 pins</td>
<td>LQFP (GJ)</td>
<td>24 x 24 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>SV1, ME2</td>
</tr>
<tr>
<td>176 pins</td>
<td>LQFP (GM)</td>
<td>24 x 24 mm</td>
<td>0.5 mm</td>
<td>1.4 mm</td>
<td>SV1, ME2</td>
</tr>
</tbody>
</table>
Performance range of 20 to over 300 MIPS with single instruction set

- Utilization of existing software resources
- Maintenance of real-time performance
- Pursuit of low power consumption

### CPU Core Function Comparison

<table>
<thead>
<tr>
<th>CPU Core Function</th>
<th>V850</th>
<th>V850ES</th>
<th>V850E1</th>
<th>V850E2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum operating frequency</td>
<td>20/33 MHz</td>
<td>20/32 MHz</td>
<td>66→100→150 MHz</td>
<td>200→266→400 MHz</td>
</tr>
<tr>
<td>Instructions</td>
<td>47</td>
<td>80</td>
<td>80</td>
<td>89</td>
</tr>
<tr>
<td>Maximum program memory space</td>
<td>16 MB</td>
<td>16 MB</td>
<td>64 MB</td>
<td>512 MB (internal 128 MB)</td>
</tr>
<tr>
<td>Maximum data memory space</td>
<td>16 MB</td>
<td>16 MB</td>
<td>256 MB</td>
<td>4 GB</td>
</tr>
</tbody>
</table>
| Higher performance | 5-stage pipeline Harvard architecture | Improved pipeline
- Non-blocking load/store instructions
- Parallel instruction execution (instruction execution in internal ROM)
- Addition of branching/load pipe
- Shift to 3-operand manipulations in 1 slot
| 7-stage pipeline
Simultaneous execution of 2 instructions with 3 pipelines that can operate independently from each other |
| High code efficiency | 2-byte instructions CISC instructions | Addition of C language compatible instructions
(Switch instruction, Call instruction, data conversion instruction, Prepare/Dispose instruction) | 32-bit branch instruction
3-operand instruction
Sum of products instruction
Bit search instruction |
| Multiplier | 16×16 bits→32 bit multiplication | 16×16 bits→32 bit operation
32×32 bits→64 bit operation
32×32 bits→64 bit operation (32 bit multiply instruction support) |
| Interrupt responsiveness | 11 to 18 clocks | 4 to 10 clocks |
**System LSI Support**

- **Use of same development methods for standard V850 Series products, ASIC microcontrollers**
  - Quick market introduction of standard products
  - System optimization through shift to system LSIs

- **CPU core development considering system LSIs**
  - Release of cores that support on-chip debugging
  - 2-stage structure consisting of 32-bit sync system bus & 16-bit async peripheral function bus
  - Large choice of peripheral function macros

- **Many supported processes and large range of required performance, and power consumption**

---

**V850E1 system configuration example**

- NPB: Peripheral I/O bus
- VSB: System bus
- VFB: Internal instruction bus
- VDB: Internal data bus

---

**V850E2 system configuration example**

- NPB: Peripheral I/O bus
- VSB: System bus
- iLB: Internal instruction bus
- dLB: Internal data bus
The V850 Series, which consists of single-chip RISC microcontrollers that use an architecture optimized for embedding, has the following features.

- 5-stage pipeline processing
- Harvard architecture
- 32 general-purpose registers
- Simple addressing
- 2-byte basic instruction set
- Support of CISC-like instructions
- Multi-status flags
- DSP function
- 32-bit barrel shifter

### 5-stage pipeline processing

The V850 Series uses a 5-stage pipeline structure (5 stages from instruction fetch to writeback) that supports simultaneous processing of 5 instructions, thus enabling the execution of almost all instructions in just one clock.

### Harvard architecture

The V850 Series uses the Harvard architecture, which is designed so that the instruction bus and data bus can operate completely independently from each other, thereby preventing pipeline operation problems and ensuring efficient instruction execution.
32 general-purpose registers

The V850 Series provides 32 general-purpose registers. Along with a hardware environment that is ideal for program execution, the development environment, including compilers, exploits these 32 registers to achieve program generation with superior code efficiency and execution performance.

The number of registers can be selected from among 22, 26, and 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which save and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.

For example, looking at the program execution time and code size changes when the number of registers used by the compiler is changed using the servo control module, we can see that the larger the number of registers, the better the program execution speed and the smaller the code size. However, from about 26 registers, the improvement in terms of execution speed and code size becomes smaller, and in the neighborhood of 32 registers, there are no more changes. This is why the V850 Series has been provided with 32 registers as the strict minimum requirement.

Software register bank

The number of registers can be selected from among 22, 26, and 32 as a compiler option to efficiently execute application programs. Unused registers can be used as a software register bank for which save and restore processing is not required during interrupt servicing or task switching, which increases the processing speed.

General-purpose register configuration

<table>
<thead>
<tr>
<th>No.</th>
<th>Register Bank</th>
<th>Application</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ZRO Register</td>
<td>Always holds '0'</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Assembler reservation</td>
<td>Used as working register for address generation</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Address/data variable register</td>
<td>Used as stack frame generation during function call</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Stack pointer</td>
<td>Used for accessing global variables in the data area</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Global pointer</td>
<td>Used as register for specifying the beginning of the text area (program code allocation)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Text pointer</td>
<td>Used for saving status during interrupt</td>
<td></td>
</tr>
<tr>
<td>6-29</td>
<td>Address/data variable register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Element pointer</td>
<td>Used as base pointer for address generation during memory access</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Link pointer</td>
<td>Used during function call by compiler</td>
<td></td>
</tr>
<tr>
<td>PC</td>
<td>Program counter</td>
<td>Holds instruction addresses during program execution</td>
<td></td>
</tr>
</tbody>
</table>

System register configuration

<table>
<thead>
<tr>
<th>No.</th>
<th>System Register Name</th>
<th>Operation Specification</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EIPCR</td>
<td>LDSR</td>
<td>Register for saving status during interrupt</td>
</tr>
<tr>
<td>1</td>
<td>EIPCSR</td>
<td>STSR</td>
<td>Register for saving status during NMI</td>
</tr>
<tr>
<td>2</td>
<td>FPSCR</td>
<td>Reserved</td>
<td>Program status word</td>
</tr>
<tr>
<td>3</td>
<td>FEPC</td>
<td>Reserved</td>
<td>Interrupt source register</td>
</tr>
<tr>
<td>4</td>
<td>ECR</td>
<td>Reserved</td>
<td>Program status word</td>
</tr>
<tr>
<td>5</td>
<td>PSW</td>
<td>Reserved</td>
<td>Program status word</td>
</tr>
<tr>
<td>16</td>
<td>CTPC</td>
<td>Reserved</td>
<td>Register for saving status during CALLT execution</td>
</tr>
<tr>
<td>17</td>
<td>CTPSW</td>
<td>Reserved</td>
<td>Register for saving status during exception/debug trap</td>
</tr>
<tr>
<td>18</td>
<td>DBPC</td>
<td>Reserved</td>
<td>CALLT base pointer</td>
</tr>
<tr>
<td>19</td>
<td>DBPSW</td>
<td>Reserved</td>
<td>CALLT base pointer</td>
</tr>
<tr>
<td>20</td>
<td>CTBP</td>
<td>Reserved</td>
<td>CALLT base pointer</td>
</tr>
<tr>
<td>6-15,21,31</td>
<td>Reserved</td>
<td>× × ×</td>
<td>Other than V850 CPU core products</td>
</tr>
</tbody>
</table>

× : Access prohibited  LDSR: Instruction to load general-purpose register contents to system register  ○ : Access enabled  STSR: Instruction to store system register contents to general-purpose register
Simple addressing

The increased amount of address calculations in the CPU in the case of complex addressing causes disturbances in the pipeline operation. As a result, address calculation becomes a bottleneck for pipeline processing and raising the frequency to increase the performance becomes difficult. The V850 Series avoids this problem by supporting only simple addressing.

Addressing mode

- **Instruction addresses**
  - Relative addressing (PC dependent)
    Add 9 signed bits or 22 signed bits of the instruction code to the program counter.
  - Register addressing (register indirect)
    Transfer the contents of the general-purpose register specified by the instruction (reg1) to the program counter (PC).

- **Operand addresses**
  - Register addressing
    Addressing that accesses the general-purpose register specified by the general-purpose specification field or a system register as an operand.
  - Immediate addressing
    Addressing of 5-bit data or 16-bit data for manipulation in the instruction code.
  - Based addressing
    Addressing that accesses memory, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) as the operand address.
  - Bit addressing
    Addressing that accesses 1 bit of 1 byte of the memory space, with the sum of the contents of the general-purpose register (reg1) and 16-bit displacement (disp16) that has been sign extended to word length as the operand address.

2-byte basic instruction set

The V850 Series employs a 2-byte instruction code to perform basic processing to enable compact program development equivalent to 16-bit CISC microcontrollers.

- Improved object efficiency through ROMization programming
  Application of 2-byte instructions to all basic processing, consisting of load, store, arithmetic/logic operations, and branching.
- To realize ease of use, restrictions on 16-bit fixed-length instructions are partially removed through incorporation of 32-bit instructions.
- Bit manipulation instructions, etc.
CISC-like instructions for embedding (bit manipulation instructions)

The V850 Series supports bit manipulation instructions suitable for flag manipulation on I/O registers, which play a large role in embedding control.

- Improvement of operability of memory mapped I/Os for control purposes
- Manipulation of any 1 bit of byte data in the memory space
- Provision of test (test1)/set (set1)/clear (clr1)/invert (not1)
- Effective for reducing object size and execution time since flags can be manipulated in 1-bit units with 1 instruction

Multi-status flags

In the V850 Series, calculation results are reflected in registers as status flags. As a result, delay branching such as can be seen in the RISC microcontrollers of other manufacturers does not occur and programs can be coded with the same feel as CISC microcontrollers.

- Easy recording with assembler
- Improved object efficiency and execution speed

DSP function

The V850 Series provides a DSP function for executing high-speed calculations and product-sum operations indispensable for digital signal processing such as image and speech processing.

- Direct data handling via general-purpose registers
- Realization of digital signal processing through general-purpose CPU
- High-speed 16-bit (V850, V850ES CPU), 32-bit (V850E1 CPU) multiply/sum-of-products (Multiply: 1 to 2 clocks, sum-of-products: 3 clocks)
- Effective for filter operations and matrix operations for feedback calculations in speed, position, and other servo control.

32-bit barrel shifter

V850 Series can realize bit manipulations frequently used during signed data and image data processing in 1 instruction per clock.

- Shifting of any number of bits (0 to 31) executable in 1 instruction per clock
  Improved execution speed/object efficiency
  Effective for extracting arbitrary bit lengths of image data and signed data (extracting code during MH/MR/MMR encoding, etc.)
The V850E1 and V850ES cores achieve high performance and higher code efficiency through the implementation of the following improvements to the V850 CPU core.

- **Non-blocking load/store**
  - Improved bus use efficiency
  - Shorter interrupt insensitivity period

- **Addition of branch/load pipes**
  - 2-clock branching
  - Parallel execution of instructions

- **Shift to 3-operand manipulations in 1 slot**

- **Addition of high-level language-compatible instructions**
  - Improved code efficiency
  - 10 to 15% improvement in object efficiency mainly when C compiler used

### Pipeline configuration

- **Master Pipeline (V850 CPU compatible)**
  - IF (Instruction fetch): Fetches instructions and increments the fetch pointer.
  - ID (Instruction decode): Decodes instructions, creates immediate data, and reads registers.
  - EX (ALU, multiplier, barrel shifter execution): Performs arithmetic/logic operations.
  - MEM (Memory access): Accesses memory of corresponding addresses.
  - WB (Writeback): Writes execution results to registers.

- **Async WB Pipeline**
  - Calculates the address of the next instruction.

### Addition of branch/load pipes

- **Pipeline operation with branch instruction**

### Parallel instruction execution (when executed by internal ROM)

### Addition of high-level language compatible instructions

The V850E1 and V850ES cores have enhanced the instruction set of the V850 core as follows.

- **switch** (2 bytes)
- **C language switch statement processing converted into instruction**
- **callt** (2 bytes)/**ctret** (4 bytes)
- **Table-reference branching**
- **Reduction of address setting code**
- **Data conversion instructions (2 bytes)**
- **char, short type cast executed with 1 instruction**
- **sxh, sxb, zxh, and zxh instructions**
- **prepare/dispose (4 bytes)**
- **Function start/end processing executed in 1 instruction**
- **unsigned Load**
- **Reduction of unsigned manipulation code**

### Non-blocking load/store

- Pipeline is stopped until MEM stage complete

- **Effective pipeline processing that uses the Async WB Pipeline when appropriate, according to the instruction.**

### Conventional (V850 CPU)

<table>
<thead>
<tr>
<th>Load instruction</th>
<th>IF</th>
<th>ID</th>
<th>EX</th>
<th>MEM</th>
<th>WB</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD instruction</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>MEM</td>
<td>WB</td>
</tr>
<tr>
<td>Next instruction</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>MEM</td>
<td>WB</td>
</tr>
</tbody>
</table>

### V850E1 CPU

<table>
<thead>
<tr>
<th>Load instruction</th>
<th>IF</th>
<th>ID</th>
<th>EX</th>
<th>MEM</th>
<th>WB</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD instruction</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>MEM</td>
<td>WB</td>
</tr>
<tr>
<td>Next instruction</td>
<td>IF</td>
<td>ID</td>
<td>EX</td>
<td>MEM</td>
<td>WB</td>
</tr>
</tbody>
</table>

* The next branch instruction code is also fetched due to the internal 32-bit bus.
V850E2 Architecture

V850E2 core features

- Real-time performance of 250 MIPS
  - Operation at over 200 MHz
- Inheritance of V850E1 performance and features
  - Upward instruction compatibility with V850E1 and V850ES cores at object level
  - Use of 7-stage pipeline
  - Parallel pipeline configuration (2 parallel superscalar)
  - 128-bit instruction fetch bus
- Support of expanding application software sizes
  - Address space (program/data) expansion
  - Strengthened cache memory support

V850E2 core Main added functions

- 32-bit relative branch instruction
  - Support of program space expansion
  - Long-distance branching performance, elimination of code efficiency losses
- 3-operand instructions (addition of target operations)
  - Higher speed processing of operations such as multiplex add/subtract (64-bit operation, saturate operation) and bit shift, contributing to higher code efficiency
- Sum-of-products instruction
  - Higher speed 32-bit sum-of-products operation (32 × 32 + 64→64 bits)
- Bit search instruction
  - Bit row change point search for run length measurement, contributing to increased speed of conversion from integers to floating decimals, etc.

V850E2 core CPU pipeline configuration

- 2 instructions simultaneously executable using 2 instruction execution units
- Instruction memory, instruction cache
- Data memory, data cache

V850E2 core CPU pipeline operation

- Execution of up to 2 instructions/clock possible (dependent on instruction set)
- Time flow
  - Instruction fetch (IF)
  - Dispatch (DP)
  - Instruction decode (ID)
  - Instruction execution (EX)
  - Address transfer (AT)
  - Data fetch (DF)
  - Writing execution result to register (WB)
- BSFT unit
- ALU unit
- MUL unit
- MEM unit
- Write back unit

Instructions executed at each clock
Memory Access Functions

**SDRAM controller**

- Products: V850E/MA1, MA2, MA3, ME2
  - SDRAM connectable without external circuit
  - CAS latency: 2, 3 supported
  - CBR (automatic) refresh: Self refresh supported

**DMA controller (provided in V850E products)**

- Products: V850E/MA1, MA2, MA3, MS1, MS2, IA1, IA2, IA3, IA4, ME2, SV2
  - Transfer targets: Memory-peripheral I/O, memory-memory
  - Transfer mode: Single, single step, block transfer
  - Transfer units: 8/16 bits
  - Transfer type: 1-cycle transfer, 2-cycle transfer
  - Number of transfers: 65536 Max.

**DMA controller (provided in V850ES products)**

- Products: V850ES/SA2, SA3, SG2, SJ2, KG1+, FG2, FJ2, µPD703229Y, 70F3229Y
  - Transfer targets: Memory-peripheral I/O, memory-memory
  - Transfer mode: Single
  - Transfer units: 8/16 bits
  - Transfer type: 2-cycle transfer
  - Number of transfers: 65536 Max.

**DMA controller (provided in V850/Sxx products)**

- Products: V850/SA1, SB1, SB2, SV1, SF1, SC1, SC2, SC3
  - Transfer targets: Internal RAM-on-chip peripheral I/O
  - Transfer mode: Single
  - Transfer units: 8/16 bits
  - Transfer clock: 4 clocks Min.
  - Number of transfers: 256 Max.
**Analog Circuits**

### ΔΣA/D converter

Products: V850ES/PM1
- High-accuracy 16-bit resolution
- Sampling frequency selector (4.340 kHz/2.170 kHz)
- Support of up to 3 lines and 4 phases through multiple input channels

### High-speed A/D converter

Products: V850E/IA3, IA4
- Simultaneous 10-bit A/D converter sampling for 2 circuits
- On-chip operational amplifier (2.5 ×5) for input level amplification
- On-chip overvoltage detection comparator

### A/D converter (multi-stage buffer type)

Products: V850E/MA1, MA3, ME2, IA1, IA2, MS1, SV2, V850/SV1, V853, etc.
- Conversion startable by software or hardware
- 8 on-chip conversion result registers (24 for SV2)
- Select/scan mode switching possible

### D/A converter

Products: V850ES/KG1, KJ1, KG1+, KJ1+, SA2, SA3, SG2, SJ2, V850E/MA3, V853
- R-2R ladder method (except for V850ES/SA2, SA3)
- R string method (V850ES/SA2, SA3 only)
- 8-bit resolution
- Operation mode: Normal mode/real-time output mode
**Timer/Counter**

- **Timer configuration during inverter control**
  - Products: V850E/IA3, IA4, MA3, V850ES/IK1
    - 0% and 100% output and 6-phase PWM output with deadtime possible
    - Switchable anytime/batch overwrite for compare register
    - A/D converter conversion start trigger generator

- **32-bit servo timer**
  - Products: V850E/SV2
    - 32-bit timer unit for servo control
    - Capture registers: 12
    - Compare registers: 2
    - External input detection circuit with 1 to 256 dividers
    - On-chip 8-bit mask timers: 2

- **Up/down counter**
  - Products: V850E/IA1, IA2, IA3, IA4, MA3, ME2
    - 16-bit 2-phase encoder input possible
    - Compare registers: 2
    - Capture/compare registers: 2

- **Real-time counter**
  - Products: V850ES/SA2, SA3, PM1
    - On-chip week, day, hour, minute, second counters
    - Counting up to 4095 periods
    - Support of interval interrupt generation at fixed intervals selectable from: 0.015625 s, 0.03125 s, 0.0625 s, 0.125 s, 0.25 s, 0.5 s, 1 s, 1 mn, 1 hr, 1 day
**Serial Interface**

- **Serial interface with automatic send/receive function**
  - Products: V850E/SV2, V850ES/KF1, KG1, KJ1, KF1+, KG1+, KJ1+
  - 32-byte internal buffer RAM
  - Automatic send/receive function
  - 1 to 32 bytes of transfer bytes specifiable
  - Transfer interval specifiable (0 to 63 clocks)
  - Single transfer/repeated transfer specifiable

**LINBus**

- **Products:** V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2
  - Low-cost 1-line network bus
  - Sync break field (SBF) send/receive possible through hardware
    (Send: 13 bits ≤ SBF ≤ 20 bits; Receive: SBF ≥ 11 bits)
  - Also generally usable as UART

- **Port configuration for LIN reception**
  - Timer output selectable as source clock
  - Any baud rate selectable
  - SBF automatic detection

**CAN**

- **Product:** V850ES/SG2, SJ2, FE2, FF2, FG2, FJ2, V850E/IA1, V850/SF1, SC3, DB1
  - CAN protocol ver. 2.0 Part B (send/receive of standard and extended frames)
  - Max. transfer rate: 500 kbps (V850/DB1 only) 1 Mbps
  - 32 message buffer

**I2EBus controller**

- **Products:** V850ES/SG2, SJ2, V850/SB2, SC2
  - Communication mode 1 supported
  - Max. transfer bytes: 32 bytes/frame
  - Max. transfer speed: Approx. 17 kbps
**USB**

**Products:** V850E/ME2
- Compliant with Universal Serial Bus Specification
- Support of 12 Mbps (full speed) transfer
- Many endpoint configurations

**SSCG function** *(Spread spectrum Frequency Synthesizer Clock Generator)*

**Products:** V850E/ME2
- EMI peak noise reduction through input frequency modulation
- Large reduction in noise countermeasure time and cost possible
- Frequency modulation rate and modulation period changeable by register setting

**ROM correction function**

**Products:** V850 core : V850/SB1, SB2, SV1, SF1, SC1, SC2, SC3
V850E, V850ES cores : V850ES/SA2, SA3, SG2, SJ2, KE1, KF1, KG1, KJ1, KE1+, KF1+, KG1+, PM1, IK1, μPD70329Y, 70F329Y, V850E/MA3, SV2, IA3, IA4
- Instructions of address to be modified inserted to replace DBTRAP instruction (JMP r0 instruction in case of V850 core), branching to 0060H (0000H in case of V850 core)
- Program modification following switch to mask ROM possible
- Modified addresses: 4 points, 8 points
  Note V850E/SA2

**Explanation of ROM correction operation**

---

**Note** JMP r0 instruction for the V850 core
**Low-voltage detection circuit (LVI)**

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2, IK1

- Detection voltage level changeable by software
- Usable instead of reset IC, contributing to lower system cost
- Detection voltage not changeable after mode transition (security protection)

**Clock monitor function**

Products: V850ES/KE1+, KF1+, KG1+, KJ1+, SG2, SJ2, µPD703229Y, 70F3229Y, V850ES/FE2, FF2, FG2, FJ2, IK1

- Monitors abnormal stops of main clock with internal Ring-Oscillator
- During abnormal stop, entire system can be set to reset status
- Prevention of destruction due to system deadlock or runaway

**On-chip debugging function**

Products: V850E/ME2ITU+, V850E/MA3+, IA4, SV2, V850ES/KJ1, KJ1+, SG2, SJ2, FE2, FF2, FG2, FJ2, µPD70F3229Y

- Realization of on-chip debugging of microcontroller with DCU (Debug Control Unit)
- Compact and low-cost PC card-type emulator
- Flash programmer function
- Integrated debugger (ID850) supported

**Boundary scan function**

Products: V850E/SV2

- Use of JTAG (Joint Test Action Group) communication specifications, IEEE1149.1 compliant
- Progressive scan of device’s external I/O pins, test data input/output possible
- Connection check of devices soldered on user board possible

---

**Note**

Trace function support is possible by using the RTE-2000-TP made by Midas Lab Co., Ltd., or PARTNER-ET II, PARTNER-J made by Kyoto Micro Computer Co., Ltd.
V850 Series Benchmark

The V850 Series realizes high speed, high performance, and high code efficiency.

Minimum instruction execution time

- V850ES/Kxx
  - 12 MHz (0.168 µs) supported for some products
  - 10 MHz (0.2 µs) supported for some products

V850 Series performance

- Performance comparison
- Code size comparison
  - NEC Electronics measurement results using sample program

Performance comparison

- V850ES-20 MHz
- A 16-bit 20 MHz
- A 16-bit 16 MHz
- B 32-bit 50 MHz

Code size comparison

- V850ES-20 MHz
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- B 32-bit 50 MHz

Low Power Consumption

Thanks to thorough energy-saving design, a superior current/performance ratio of 1.1 to 0.7 mA/MIPS is realized, particularly for V850ES and V850/Sxx products. As a result, a reduction in power consumption to 1/5 or less compared to 16-bit CISC microcontrollers of similar performance is realized. Lower system power consumption and higher performance are simultaneously realized through this extremely high power performance.

Power performance

- 8-bit CISC: 9.2 mA/MIPS
- 16-bit CISC: 7.3 mA/MIPS
- V850/SV1: 1.1 mA/MIPS
- V850/SB1: 0.9 mA/MIPS
- V850/SA1: 0.7 mA/MIPS

Realization of low consumption current that is 1/5 or less compared to 16-bit CISC of similar performance

Clock gear function

- Reduction to 1/400 through switch from main clock to subclock
- Reduction to 1/10th through clock gear (1/32)
- Reduction to 1/5th through clock gear (1/8)

Standby mode

- Normal operation mode
- HALT mode
- IDLE mode
- Sub normal operation mode
- Sub IDLE mode
- STOP mode (sub operations)
- STOP mode (sub stop)

Consumption current

- Operating
- Stopped

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- Normal operation mode
- HALT mode
- IDLE mode
- Sub normal operation mode
- Sub IDLE mode
- STOP mode (sub operations)
- STOP mode (sub stop)

Consumption current

- Operating
- Stopped
Minimizing the influence of electromagnetic interference (EMI) emitted from the microcontroller and the influence of noise applied to the microcontroller (EMS) is a high priority, particularly for AV equipment such as car audio systems, and thus superior noise performance is required of microcontrollers. Various noise countermeasures are implemented in the V850 Series, and noise performance equivalent or superior to that of 16-bit products has been realized.

### EMS countermeasures

- Use of PLL for oscillation circuit
- Voltage control oscillator
- Oscillation circuit
- LPF
- VCO
- divider
- To CPU peripheral functions
- High-frequency noise cut through PLL filter

### EMS measurement results (power supply coupling measurement)

<table>
<thead>
<tr>
<th>Noise application voltage</th>
<th>0 kV</th>
<th>1.0 kV</th>
<th>2.0 kV or higher</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850ES/KJ1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Existing V850 products</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(PLL-less products)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>V850ES/KJ1 (flash version)</th>
<th>Existing V850 products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc=5 V</td>
<td>Vcc=5 V</td>
</tr>
<tr>
<td>Resonator: 4 MHz</td>
<td>Resonator: 16 MHz</td>
</tr>
<tr>
<td>Internal operation frequency: 16 MHz</td>
<td>Internal operation frequency: 16 MHz</td>
</tr>
</tbody>
</table>

### EMI noise countermeasures: Power supply circuit countermeasures

- CPU power supply separation
- Insertion of capacitance between VDD and GND
- Port power supply separation
- Due to the relation between the power supply and GND pad positions and the lead frame, placement is done so as to lower the power supply impedance.

### EMS noise measurement results

- Power supply voltage: 5V
- Operating frequency: 78K0 10MHz
- V850ES/KJ1 16MHz
- Existing 78K0
- V850ES/KJ1

- Frequency [MHz]
- Noise [dBm]
Next-generation processors
V850 Series

RISC

Platforms

Planning
System design
Development
Mass production

Original NEC
IP vendors
Standards

Middleware plays a major role for maximizing processor performance and realizing high-speed processing of complex data with flexibility and ease.

NEC Electronics offers a large array of middleware that is optimized for the CPU architecture and importantly contributes to shortening development time, while also facilitating additions and changes to dedicated functions whose implementation as hardware for devices, etc., used to have high cost and time requirements, and the creation of user-friendly interfaces.

Middleware merits:
- Shortening of development time
- Reduction in development cost
- Realization of latest technology and functions
- Easy performance enhancement and function expansion
- Easy creation of user-friendly interface
- Multimedia processing realizable just with CPU
- Realization of higher reliability and quality

Maximization of system added value

Shift to middleware accelerating deployment to optimum processors

An increasing number of processors optimized for various systems and based on NEC Electronics' original technology and the superb technology of third parties, as well as other technologies that have been established as standards, are being deployed from.

Middleware product list

<table>
<thead>
<tr>
<th>Category</th>
<th>Middleware</th>
<th>V850 Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image</td>
<td>JPEG</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MPEG-4/H.263 Video</td>
<td></td>
</tr>
<tr>
<td>Speech</td>
<td>Text To Speech</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Japanese</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Speech CODEC</td>
<td></td>
</tr>
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Middleware performance list

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<th>RAM</th>
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<td>JPEG</td>
<td>QVGA×24 : Enc0.32s/Dec0.24s</td>
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<td>17.5 KB</td>
<td>15 KB</td>
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<tr>
<td>G.726 (ADPCM)</td>
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<td>En0/Dec8.2</td>
<td>9 KB</td>
<td>60 B</td>
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<tr>
<td>Speech recognition (small vocabulary)</td>
<td>0.4s</td>
<td>—</td>
<td>82 KB</td>
<td>3.5 KB</td>
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<tr>
<td></td>
<td>(100 words)</td>
<td>—</td>
<td>(15 words)</td>
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</table>
Speech Recognition

Speech recognition is realized on a single chip using the memory and peripheral I/Os in the V850 Series. Ideal for applications such as games and home appliances that must feature speech recognition but are subject to large restrictions.

- Realization of speech recognition with memory and peripheral I/Os contained in V850 Series
- Expansion of number of recognized words

Recognized number of words: 30 words (in case of V850/SA1, 20 MHz)

JPEG

- Conforms to JPEG international standard
- Conforms to DCT baseline process (non-reverse coding)
- Versatile compression and decompression processing

<Compression functions>
- User-customizable VRAM input module
- User-specified Huffman and quantization tables
- APPn marker insertion
- Compression suspend function

<Decompression processing>
- User-customizable VRAM output module
- Support of various JPEG markers (DRI, RSTn, DNL)
- Decompression suspend function

Text to Speech (for Japanese Text)

- Speech synthesized from Japanese Kana and Kanji text (SJIS code)
- Versatile speech synthesis
  - Synthesis of female voices possible
  - Various adjustable parameters such as intonation and reading speed
  - Rhythm of synthesized speech (pitch, phoneme duration) can be designed (Speech Designer compatible)
  - Speech synthesis using natural rhythm possible (synthesis of more natural sounding speech)
  - Support of special characters (Reading of special characters settable in user dictionaries)
  - Synthesis speed

Works also with V850/SA1 (20 MHz). (However, text is placed in internal ROM.)
To answer the need for shorter development time and maintenance after shipping, NEC Electronics offers microcontrollers with on-chip flash memory available in a large range of capacities from 64 KB to 640 KB as part of the V850 Series. NEC Electronics’ flash memory microcontrollers offer the following features.

- Flash capacity
  64 to 640 KB
- Overwrite unit
  Entire memory at one time, or block units
- Rewrite method
  Serial communication with dedicated flash memory programmer (on-board, off-board)
- Self-flash programming
- Rewrite voltage
  Single-power-supply flash: Operation voltage
  Dual-power-supply flash: Operation voltage
  7.8 V/10.3 V
- Rewrite count:
  100 times

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<tr>
<th>Flash Memory Size (bytes)</th>
<th>64K</th>
<th>128K</th>
<th>192K</th>
<th>256K</th>
<th>384K</th>
<th>512K</th>
<th>64K</th>
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<td>RAM size (bytes)</td>
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<td>8K</td>
<td>16K</td>
<td>16K</td>
<td>16K</td>
<td>24K</td>
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Features

Rewrite Modes

To enable integrated use ranging from development to mass production and maintenance, the V850 Series supports a programmer rewrite mode that uses serial communication supporting on-board programming, as well as a self-programming mode that rewrites flash memory with user programs.

- On-board programming mode
  This programming mode is used to rewrite the flash memory mounted on the target system using a dedicated flash memory programmer.
- Off-board programming mode
  This programming mode is used to rewrite flash memory using a dedicated flash memory programmer and dedicated program adapter (FA Series).
- Self-programming mode
  This programming mode is used to rewrite flash memory by executing the user program written beforehand to the flash memory using on-board/off-board programming.

Notes 1. The FA Series is a product of Naito Densei Machida Mfg. Co., Ltd.
2. Since instruction fetch and data access cannot be performed from the internal flash memory area during self-programming, a program for rewriting internal RAM or external memory must be transferred in advance.

Programmer program (on-board/off-board)

Note 1. In the case of dual-power-supply flash, VPP don’t connect.
Flash memory can be erased and rewritten using a self-programming library from a program placed in an area outside the flash memory.

### Flash Specifications List

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<tr>
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<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>√</td>
<td>√</td>
<td>100</td>
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<tr>
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<td>V850ES/KF1</td>
<td>256 KB/128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>√</td>
<td>√</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>V850ES/KE1</td>
<td>128 KB</td>
<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>√</td>
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<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>√</td>
<td>√</td>
<td>100</td>
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<tr>
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<td>V850ES/KG1</td>
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<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
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<td>4.5 V to 5.5 V</td>
<td>√</td>
<td>√</td>
<td>100</td>
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<td>20 MHz</td>
<td>4.5 V to 5.5 V</td>
<td>√</td>
<td>√</td>
<td>100</td>
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<tr>
<td></td>
<td>V850/SC1</td>
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<td>20 MHz</td>
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<td>100</td>
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<td>V850/SK2</td>
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</tbody>
</table>

*: Under development
Flash Memory Programmers

NEC Electronics flash memory programmer: PG-FP4

[Features]
- Supports write to all NEC Electronics microcontrollers with internal flash memory.
- USB support through host machine interface
- Allows verification of various types of information, including programmer setting information, error messages, and check-sum, even in stand-alone configuration, from the main unit's LCD.
- Enables downloading of two types of user code and selecting of valid code
- Device-specific information required for writing automatically settable with parameter files
- Supports both on-board programming and program adapter programming.
- Easy-to-carry A5 size
- Simple operation either on stand-alone basis and on Windows™ 95/Windows 98/Windows Me/ Windows 2000/Windows XP, Windows NT™ 4.0 using a dedicated application (Flashpro4)

Flash memory programmer configuration
PG-FP4 allows single-microcontroller programming when used with a program adapter (FA Series of Naito Densei Machida Mfg. Co., Ltd.). On-board programming can also be performed.

A sample rewrite environment when using the program adapter is shown below.

Rewrite environment example

Third-party flash memory programmers (1/2)

Programming system Y1000-8

[Manufacturer/Distributor] Wave Technology Co., Ltd.
[Target Devices] V850/SV1, SB1 (µPD70F3032B, 70F3033B), SB2 (70F3035B, 70F3037H), V850EIA1 (70F3116), MA1

[Features]
- Gang programmer enabling simultaneous programming and verification of up to 8 devices
- Enables reading of master data directly from floppy disk to internal memory
- Data dump display and editing functions
- Master data storable on internal hard disk
- Designed for simple and comfortable operation via touch panel, and superior operability via PASS/FAIL display, check-sum display, and task count display supporting sockets.

[Additional information]
TEL : +81-3-5304-1885  FAX : +81-3-5304-1886
E-mail : sales@y1000.com
Website: http://www.y1000.com/index_e.html

Cautions 1. Install the PG-FP4 control software and target device parameter file in the host machine.
- PG-FP4 control software: Bundled with PG-FP4
- PG-FP4 parameter file: Distributed via online delivery service

2. In addition to programming using the program adapter, on-board programming on the target system is also possible.
Third-party flash memory programmers (2/2)

FlashPRO IV: FL-PR4
[Target Devices] V850 Series
[Features]
- Supports writing to all NEC Electronics microcontrollers with internal flash memory.
- USB support through host machine interface.
- Allows verification of various types of information, including programmer setting information, error messages, and checksum, even in standalone configuration, from the main unit’s LCD.
- Enables downloading of two types of user code and selecting of valid code.
- Device-specific information required for writing automatically settable with parameter files.
- Supports both on-board programming and program adapter programming.
- Easy-to-carry A5 size.
- Simple operation either on stand-alone basis and on Windows 95/Windows 98/Windows Me/Windows 2000/Windows XP/Windows NT 4.0 using a dedicated application (Flashpro4).
[Additional Information]
TEL: +81-45-475-4191 FAX: +81-45-475-4091
E-mail: info@ndk-m.co.jp
Website: http://www.ndk-m.co.jp/asmis/eng/index.html

NET IMPRESS
[Manufacturer/Distributor] Yokogawa Digital Computer Corporation
[Target Devices] V850/SB1 (µP70F3033B), SB2(70F3037H), SA1(70F3017A), SC3(70F3089Y), V853(70F3033A, 70F3025A), V856E/MS1(70F3312), MA1(70F3107), (A1, IA2(70F3114), V856ES/KE1(70F3210), FE2, FF2, F32, FG2, SG2, SJ2)
[Features]
- Enables programming of flash memory microcontrollers of various writing specifications solder mounted on user system boards.
- One control module is the key to this product’s versatility. Microcontrollers of the same family are supported by changing parameters, and microcontrollers of different families are supported by purchasing the required license for the descriptor part.
- Can be used on standalone basis as well as via a host machine.
- Rich lineup of downloadable freeware.
[Additional Information]
TEL: Japan +81-42-333-6224
U.S.A +408-941-0132 (Yokogawa Corporation of America)
Europe +44-1256-811791 (Ashling Microsystems Limited)
Korea +82-2-785-3929 (KM DATA INC.)
South East Asia +65-6563-2082 (Unidux Electronics Pte Ltd.)
FAX: Japan +81-42-352-6109
U.S.A +408-941-0121 (Yokogawa Corporation of America)
Europe +44-1256-811791 (Ashling Microsystems Limited)
Korea +82-2-785-3117 (KM DATA INC.)
South East Asia +65-6569-4661 (Unidux Electronics Pte Ltd.)
Website: http://www.ydc.co.jp/micom/index_E.htm

Flash Burner Forward FL-S01, Flash Gang Forward FL-G01
[Manufacturer] Forward Electric Co., Ltd. (Hong Kong)
[Distributor] Application Co., Ltd.
[Target Devices] V850/SB1(70F3033A), V856E/MA1
[Features]
- Host machine interface supports USB.
- Easy operation and rich array of GUI software provided.
- Low cost from development to mass production.
- Compact and easy to carry (FL-S01).
- Gang programmer enabling simultaneous programming of up to 8 devices (FL-G01).
- Can be used on standalone basis using compact flash (FL-G01).
- Programming adapter board (option) usable in common for FL-S01 and FL-G01.
[Additional Details]
Website: http://www.apply.co.jp/index_eng.html
### Low-End Lineup (1/2)

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<th>Item</th>
<th>( \mu P D 7 0 3 2 0 7 / 3 2 0 7 Y )</th>
<th>( \mu P D 7 0 3 2 0 7 / 3 2 0 7 H )</th>
<th>( \mu P D 7 0 3 2 0 8 / 3 2 0 8 Y )</th>
<th>( \mu P D 7 0 3 2 0 8 / 3 2 0 8 H )</th>
<th>( \mu P D 7 0 3 2 1 0 / 3 2 1 0 Y )</th>
<th>( \mu P D 7 0 3 2 1 0 / 3 2 1 0 H )</th>
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<td>( \mu P D 7 0 3 2 0 7 / 3 2 0 7 H / 3 2 1 0 / 3 2 1 0 H )</td>
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<td>( \mu P D 7 0 3 2 0 8 / 3 2 0 8 H / 3 2 1 0 H )</td>
<td>( \mu P D 7 0 3 2 1 0 / 3 2 1 0 Y / 3 2 1 0 H )</td>
<td>( \mu P D 7 0 3 2 1 0 / 3 2 1 0 H )</td>
</tr>
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<td>29 MIPS (2/16 MHz: 1/2 Mhz)</td>
<td>29 MIPS (2/16 MHz: 1/2 Mhz)</td>
<td>29 MIPS (2/16 MHz: 1/2 Mhz)</td>
<td>29 MIPS (2/16 MHz: 1/2 Mhz)</td>
<td>29 MIPS (2/16 MHz: 1/2 Mhz)</td>
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<tr>
<td>Peripheral functions</td>
<td>I2C interface, Serial interface, Watchdog timer, Memory controller, Ports I/O, DMA controller, A/D converter, External bus interface, Interrupt sources, Debug control unit, Other peripheral functions, Operating ambient temperature</td>
<td>I2C interface, Serial interface, Watchdog timer, Memory controller, Ports I/O, DMA controller, A/D converter, External bus interface, Interrupt sources, Debug control unit, Other peripheral functions, Operating ambient temperature</td>
<td>I2C interface, Serial interface, Watchdog timer, Memory controller, Ports I/O, DMA controller, A/D converter, External bus interface, Interrupt sources, Debug control unit, Other peripheral functions, Operating ambient temperature</td>
<td>I2C interface, Serial interface, Watchdog timer, Memory controller, Ports I/O, DMA controller, A/D converter, External bus interface, Interrupt sources, Debug control unit, Other peripheral functions, Operating ambient temperature</td>
<td>I2C interface, Serial interface, Watchdog timer, Memory controller, Ports I/O, DMA controller, A/D converter, External bus interface, Interrupt sources, Debug control unit, Other peripheral functions, Operating ambient temperature</td>
<td>I2C interface, Serial interface, Watchdog timer, Memory controller, Ports I/O, DMA controller, A/D converter, External bus interface, Interrupt sources, Debug control unit, Other peripheral functions, Operating ambient temperature</td>
</tr>
</tbody>
</table>

Notes: 1. Number of external interrupts that can be used to release STOP mode
2. Only 3 products have an on-chip I2C interface.
3. \( \mu P D 7 0 3 2 1 0 / 3 2 1 0 H \) is only.

### Notes
- **Power consumption (Typ.):**
  - 293.7 mW (296 KB products: 20 MHz @ 3.3 V operation)
  - 290.7 mW (32 KB mask products: 20 MHz @ 3.3 V operation)
- **Package:**
  - 80-pin QFP (10 mm)
### Low-End Lineup (2/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/KR1+</th>
<th>V850ES/KR1-</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD70F3311F/3311Y</td>
<td>µPD70F3316F/3316Y</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850ES</td>
<td>V850ES</td>
</tr>
<tr>
<td>CPU performance</td>
<td>29 MIPS (500 MHz; 5 MHz × 6)</td>
<td>29 MIPS (500 MHz; 5 MHz × 6)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (flash)</td>
<td>128 KB (flash)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>8 KB</td>
<td>16 KB</td>
</tr>
<tr>
<td>External interface</td>
<td>Bus type</td>
<td>Multiplexed/separate</td>
</tr>
<tr>
<td></td>
<td>Address bus</td>
<td>32 bits</td>
</tr>
<tr>
<td></td>
<td>Data bus</td>
<td>24 bits</td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>41 (Y products: 42)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>Using main clock: 2 to 20 MHz</td>
<td>Using main clock: 2 to 20 MHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>200 mW (128 KB mask products: 20 MHz @ 5 V operation)</td>
<td>220 mW (256 KB mask products: 20 MHz @ 5 V operation)</td>
</tr>
<tr>
<td>Package</td>
<td>64-pin TQFP (12 x 12 mm)</td>
<td>80-pin QFP (16 x 16 mm)</td>
</tr>
</tbody>
</table>

### Notes:
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface
3. These UARTs are the identical and the number of channels in KJ1+ totals 3 channels.

---

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/KR1+</th>
<th>V850ES/KR1-</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD70F3302/3302Y</td>
<td>µPD70F3306F/3306Y</td>
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<tr>
<td>CPU core</td>
<td>V850ES</td>
<td>V850ES</td>
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<tr>
<td>CPU performance</td>
<td>29 MIPS (500 MHz; 5 MHz × 6)</td>
<td>29 MIPS (500 MHz; 5 MHz × 6)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (flash)</td>
<td>128 KB (flash)</td>
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<td>Internal RAM</td>
<td>4 KB</td>
<td>6 KB</td>
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<td>External interface</td>
<td>Bus type</td>
<td>Multiple</td>
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<td></td>
<td>Address bus</td>
<td>16 bits</td>
</tr>
<tr>
<td></td>
<td>Data bus</td>
<td>16 bits</td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>28 (Y products: 27)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>89/29 MIPS</td>
<td>89/29 MIPS</td>
</tr>
<tr>
<td>Power consumption</td>
<td>59.4 mW (128 KB flash products: 10 MHz @ 3.3 V operation)</td>
<td>220 mW (128 KB mask products: 20 MHz @ 5 V operation)</td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 20 mm)</td>
</tr>
</tbody>
</table>

### Notes:
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip I²C interface
3. These UARTs are the identical and the number of channels in K1+ totals 3 channels.
Notes 1. Only products without IEBus or aFCAN

1. Only products without IEBus or aFCAN

2. Only products with IEBus or aFCAN

3. Only products with two aFCAN channels

4. Number of external interrupts that can be used to release STOP mode

5. Only Y products have an on-chip I2C interface.

6. Only products with external I2C interface

7. Only products with external bus

8. Part No. and volume of internal RAM and ROM

9. Operating ambient temperature

10. Power consumption (Typ.)

11. Power supply voltage

12. Operating frequency

13. Ports I/O

14. DMA controller

15. Debug control unit

16. Other peripheral functions

17. CPU performance

18. CPU core

19. Item

20. Power supply voltage

21. Package

22. Power consumption (Typ.)

23. Power supply voltage

24. Operating frequency

25. Ports I/O

26. DMA controller

27. Debug control unit

28. Other peripheral functions

29. CPU performance

30. CPU core

31. Item

32. Power supply voltage

33. Package

34. Power consumption (Typ.)

35. Power supply voltage

36. Operating frequency

37. Ports I/O

38. DMA controller

39. Debug control unit

40. Other peripheral functions

41. CPU performance

42. CPU core

43. Item

44. Power supply voltage

45. Package

46. Power consumption (Typ.)

47. Power supply voltage

48. Operating frequency

49. Ports I/O

50. DMA controller

51. Debug control unit

52. Other peripheral functions

53. CPU performance

54. CPU core

55. Item

56. Power supply voltage

57. Package

58. Power consumption (Typ.)

59. Power supply voltage

60. Operating frequency

61. Ports I/O

62. DMA controller

63. Debug control unit

64. Other peripheral functions

65. CPU performance

66. CPU core

67. Item

68. Power supply voltage

69. Package

70. Power consumption (Typ.)

71. Power supply voltage

72. Operating frequency

73. Ports I/O

74. DMA controller

75. Debug control unit

76. Other peripheral functions

Notes 5. Only products with external I2C interface

Notes 6. Only products with external bus

Notes 7. Only products with external I2C interface

Notes 8. Only products with external bus

Notes 9. Only products with external I2C interface

Notes 10. Only products with external bus

Notes 11. Only products with external I2C interface

Notes 12. Only products with external bus

Notes 13. Only products with external I2C interface

Notes 14. Only products with external bus

Notes 15. Only products with external I2C interface

Notes 16. Only products with external bus

Notes 17. Only products with external I2C interface

Notes 18. Only products with external bus

Notes 19. Only products with external I2C interface

Notes 20. Only products with external bus

Notes 21. Only products with external I2C interface

Notes 22. Only products with external bus

Notes 23. Only products with external I2C interface

Notes 24. Only products with external bus

Notes 25. Only products with external I2C interface

Notes 26. Only products with external bus

Notes 27. Only products with external I2C interface

Notes 28. Only products with external bus

Notes 29. Only products with external I2C interface

Notes 30. Only products with external bus

Notes 31. Only products with external I2C interface

Notes 32. Only products with external bus

Notes 33. Only products with external I2C interface

Notes 34. Only products with external bus

Notes 35. Only products with external I2C interface

Notes 36. Only products with external bus

Notes 37. Only products with external I2C interface

Notes 38. Only products with external bus

Notes 39. Only products with external I2C interface

Notes 40. Only products with external bus

Notes 41. Only products with external I2C interface

Notes 42. Only products with external bus

Notes 43. Only products with external I2C interface

Notes 44. Only products with external bus

Notes 45. Only products with external I2C interface

Notes 46. Only products with external bus

Notes 47. Only products with external I2C interface

Notes 48. Only products with external bus

Notes 49. Only products with external I2C interface

Notes 50. Only products with external bus

Notes 51. Only products with external I2C interface

Notes 52. Only products with external bus

Notes 53. Only products with external I2C interface

Notes 54. Only products with external bus

Notes 55. Only products with external I2C interface

Notes 56. Only products with external bus

Notes 57. Only products with external I2C interface

Notes 58. Only products with external bus

Notes 59. Only products with external I2C interface

Notes 60. Only products with external bus

Notes 61. Only products with external I2C interface

Notes 62. Only products with external bus

Notes 63. Only products with external I2C interface

Notes 64. Only products with external bus

Notes 65. Only products with external I2C interface

Notes 66. Only products with external bus

Notes 67. Only products with external I2C interface

Notes 68. Only products with external bus

Notes 69. Only products with external I2C interface

Notes 70. Only products with external bus

Notes 71. Only products with external I2C interface

Notes 72. Only products with external bus

Notes 73. Only products with external I2C interface

Notes 74. Only products with external bus

Notes 75. Only products with external I2C interface

Notes 76. Only products with external bus
Middle-Range Lineup (2/3)

### Item

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>µPD703229Y</td>
<td>µPD700068Y</td>
<td>µPD700069Y</td>
<td>µPD703088Y</td>
<td>µPD703089Y</td>
<td>µPD703088Y</td>
<td>µPD703089Y</td>
<td>µPD703089Y</td>
<td>µPD708089Y</td>
</tr>
<tr>
<td>CPU performance</td>
<td>V850</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 19 MHz)</td>
<td>18 MIPS (@ 16 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>384 KB (mask)</td>
<td>384 KB (flash)</td>
<td>512 KB (mask)</td>
<td>512 KB (flash)</td>
<td>384 KB (mask)</td>
<td>384 KB (flash)</td>
<td>512 KB (mask)</td>
<td>512 KB (flash)</td>
<td>384 KB (mask)</td>
</tr>
<tr>
<td>External bus interface</td>
<td>Bus type</td>
<td>Multiplexed/separate</td>
<td>Multiplexed (can be separated only for V850/SC1, V850/SC2)</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
<td>Multiplexed</td>
</tr>
<tr>
<td>Address bus</td>
<td>18 bits</td>
<td>22 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
</tr>
<tr>
<td>Data bus</td>
<td>8/16 bits</td>
<td>22 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
<td>18 bits</td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>32 sources</td>
<td>42</td>
<td>44</td>
<td>46</td>
<td>49</td>
<td>42</td>
<td>44</td>
<td>46</td>
</tr>
<tr>
<td>Ports I/O</td>
<td>84</td>
<td>512</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>128</td>
<td>128</td>
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<tr>
<td>Power supply voltage</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
<td>3.3 to 5.5 V</td>
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<tr>
<td>Power consumption (Typ.)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
<td>100 mW (5 V, @ 20 MHz)</td>
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<tr>
<td>Package</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
<td>100-pin LQFP (14 x 14 mm)</td>
</tr>
</tbody>
</table>

### Notes

1. Number of external interrupts that can be used to release STOP mode
2. Only I products have an on-chip I2C interface

---

**Power Consumption**

- 125 mW (5 V, @ 20 MHz)
- 165 mW (5 V, @ 20 MHz)
- 125 mW (5 V, @ 20 MHz)
- 125 mW (5 V, @ 20 MHz)
- 165 mW (5 V, @ 20 MHz)
- 125 mW (5 V, @ 20 MHz)
- 210 mW (5 V, @ 20 MHz)

*Operating ambient temperature: -40 to +85°C*
## Middle-Range Lineup (3/3)

<table>
<thead>
<tr>
<th>Item</th>
<th>V850ES/S32</th>
<th>V850ES/S33</th>
<th>V850ES/S34</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part No.</td>
<td>µPD703200/3201Y</td>
<td>µPD703201/3201Y</td>
<td>µPD703202/3202Y</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850ES</td>
<td>V850ES</td>
<td>V850ES</td>
</tr>
<tr>
<td>CPU performance</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>29 MIPS (@ 20 MHz)</td>
<td>29 MIPS (@ 20 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (mask) 256 KB (mask) 256 KB (flash) 256 KB (mask) 256 KB (flash)</td>
<td>ROM-less</td>
<td></td>
</tr>
<tr>
<td>Internal RAM</td>
<td>8 KB</td>
<td>8 KB</td>
<td>8 KB</td>
</tr>
<tr>
<td>External bus</td>
<td>Multiplexed/separate</td>
<td>Separate/multiplexed (selectable only for CSI1)</td>
<td>Multiplexed/separate</td>
</tr>
<tr>
<td>Interface</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus type</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address bus</td>
<td>22 bits</td>
<td>24 bits</td>
<td>22 bits</td>
</tr>
<tr>
<td>Data bus</td>
<td>8/16 bits</td>
<td>8/16 bits</td>
<td>8/16 bits</td>
</tr>
<tr>
<td>Chip select signal</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAAM, etc.</td>
<td>SRAAM, etc.</td>
<td>SPOAM, etc.</td>
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<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>Internal</td>
<td>Internal</td>
</tr>
<tr>
<td>Chip select signal</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<tr>
<td>External</td>
<td>8 (8/16/32)</td>
<td>8 (8/16/32)</td>
<td>8 (8/16/32)</td>
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<td>Interface</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Timer/counter</td>
<td>16-bit timer/event counter = 2 ch 8-bit timer/event counter = 4 ch</td>
<td>16-bit timer/event counter = 1 ch 8-bit timer/event counter = 4 ch</td>
<td></td>
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<tr>
<td>Watchdog timer</td>
<td>3 ch</td>
<td>3 ch</td>
<td>3 ch</td>
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<tr>
<td>Serial interface</td>
<td>CSI = 2 ch</td>
<td>CSI = 3 ch</td>
<td>CSI = 1 ch</td>
</tr>
<tr>
<td></td>
<td>CSI/UART = 1 ch</td>
<td>CSI/UART = 1 ch</td>
<td>CSI/UART = 1 ch</td>
</tr>
<tr>
<td></td>
<td>CSI/PC = 1 ch</td>
<td>CSI/UART = 1 ch</td>
<td>CSI/UART = 1 ch</td>
</tr>
<tr>
<td>A/D converter</td>
<td>10-bit = 12 ch 10-bit = 16 ch 10-bit = 8 ch</td>
<td>8-bit = 2 ch</td>
<td></td>
</tr>
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<td></td>
<td>10-bit = 16 ch</td>
<td>10-bit = 16 ch</td>
<td>10-bit = 16 ch</td>
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<tr>
<td>D/A converter</td>
<td>8-bit = 1 ch</td>
<td>8-bit = 2 ch</td>
<td>8-bit = 2 ch</td>
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<td></td>
<td>8-bit = 2 ch</td>
<td>8-bit = 2 ch</td>
<td>8-bit = 2 ch</td>
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<tr>
<td>DMA controller</td>
<td>4 ch</td>
<td>4 ch</td>
<td>4 ch</td>
</tr>
<tr>
<td>Ports</td>
<td>68</td>
<td>64</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td>Input</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>Debug control unit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other peripheral functions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROM correction function</td>
<td>4 points, real-time counter (watch timer): 1 ch</td>
<td>Real-time output</td>
<td></td>
</tr>
<tr>
<td>Operating frequency</td>
<td>When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz</td>
<td>20 to 34 MHz</td>
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<tr>
<td>Power supply voltage</td>
<td>2.2 to 2.7 V</td>
<td>3.0 to 3.6 V</td>
<td>3.0 to 3.6 V</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>38 mW (2.5 V, @ 20 MHz) 46 mW (2.5 V, @ 20 MHz) 38 mW (2.5 V, @ 20 MHz)</td>
<td>66 mW (3.3 V, @ 20 MHz)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>46 mW (2.5 V, @ 20 MHz)</td>
<td>99 mW (3.0 V, @ 17 MHz)</td>
<td>99 mW (3.0 V, @ 17 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>100-pin TQFP (14 x 14 mm)</td>
<td>121-pin FBGA (12 x 12 mm)</td>
<td>121-pin FBGA (12 x 12 mm)</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

Notes:
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip PC interface.

## Item

<table>
<thead>
<tr>
<th>Part No.</th>
<th>µPD703174A/3017AY</th>
<th>µPD703175B/3017BY</th>
<th>µPD703176B/3017BY</th>
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</thead>
<tbody>
<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
<td>V850</td>
</tr>
<tr>
<td>CPU performance</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
<td>23 MIPS (@ 20 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>64 KB (mask) 128 KB (mask) 128 KB (flash) 256 KB (mask) 256 KB (flash)</td>
<td>8 KB</td>
<td></td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB</td>
<td>8 KB</td>
<td>8 KB</td>
</tr>
<tr>
<td>External bus</td>
<td>Multiplexed/separate</td>
<td>Multiplexed/separate</td>
<td>Multiplexed/separate</td>
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<td>Interface</td>
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</tr>
<tr>
<td>Bus type</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Address bus</td>
<td>22 bits</td>
<td>16 bits</td>
<td>16 bits</td>
</tr>
<tr>
<td>Data bus</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Chip select signal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAAM, etc.</td>
<td></td>
<td></td>
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<td>Interrupt sources</td>
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<td>Timer/counter</td>
<td>16-bit timer/event counter = 2 ch 8-bit timer/event counter = 4 ch</td>
<td>16-bit timer/event counter = 2 ch 8-bit timer/event counter = 4 ch</td>
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<td>Watchdog timer</td>
<td>1 ch</td>
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<td>10-bit = 12 ch</td>
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<td>10-bit = 16 ch</td>
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<td>8-bit = 2 ch</td>
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<td>DMA controller</td>
<td>3 ch (dedicated internal RAM+on-chip peripheral I/O)</td>
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<td>Ports</td>
<td>68</td>
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<td>Input</td>
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<td>Debug control unit</td>
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<td>Other peripheral functions</td>
<td>Watch timer: 1 ch</td>
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<tr>
<td>Operating frequency</td>
<td>When using main clock: 2 to 20 MHz When using subclock: 32.768 kHz</td>
<td>20 to 34 MHz</td>
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<td>Power supply voltage</td>
<td>3.0 to 3.6 V</td>
<td>3.0 to 3.6 V</td>
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<td>Power consumption (Typ.)</td>
<td>66 mW (3.3 V, @ 20 MHz) 56 mW (3.0 V, @ 17 MHz) 105 mW (3.3 V, @ 20 MHz)</td>
<td>66 mW (3.3 V, @ 20 MHz)</td>
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<td>99 mW (3.0 V, @ 17 MHz)</td>
<td>105 mW (3.3 V, @ 20 MHz)</td>
<td>99 mW (3.0 V, @ 17 MHz)</td>
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<td>Package</td>
<td>121-pin FBGA (12 x 12 mm) 100-pin LOFQ (14 x 14 mm) 121-pin FBGA (12 x 12 mm)</td>
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<tr>
<td>Operating ambient temperature</td>
<td>-40°C to +85°C</td>
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Notes:
1. Number of external interrupts that can be used to release STOP mode
2. Only Y products have an on-chip PC interface.
### ASSP Lineup (1/3)

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<tr>
<th>Item</th>
<th>μPD703185</th>
<th>μPD703186</th>
<th>μPD70F3186</th>
<th>μPD703116</th>
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<td>V86E1</td>
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<td>CPU performance</td>
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<td>82 MIPS (56 MHz)</td>
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### ASSP Lineup (2/3)

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<th>V800ES/FE2</th>
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<td>Interrupt sources</td>
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<td>External: 9/5/8/16/32</td>
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<td>16-bit timer/event counter (TMM) = 4 ch</td>
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<td>16-bit interval timer (TMM) = 1 ch</td>
<td>16-bit interval timer (TMM) = 1 ch</td>
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<tr>
<td>Watching timer</td>
<td>1 ch</td>
<td>1 ch</td>
</tr>
<tr>
<td>Serial interface</td>
<td>CSI = 2 ch</td>
<td>UART (LIN compatible) = 2 ch</td>
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<tr>
<td></td>
<td>UART (LIN compatible) = 2 ch</td>
<td>UART (LIN compatible) = 2 ch</td>
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<tr>
<td>ADC converter</td>
<td>10-bit = 16 ch</td>
<td>10-bit = 12 ch</td>
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<tr>
<td>DMA controller</td>
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<tr>
<td>Ports</td>
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<td>128×16</td>
<td>83</td>
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<td>Debug control unit</td>
<td>–</td>
<td>Provided (RUN, break)</td>
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<td>Provided (RUN, break)</td>
<td>Provided (RUN, break)</td>
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<td>Provided (RUN, break)</td>
<td>Provided (RUN, break)</td>
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<tr>
<td>Other peripheral functions</td>
<td>Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 1 ch</td>
<td>Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 1 ch</td>
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<td>When using main clock: 16 to 20 MHz</td>
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<td>Power consumption (Typ.)</td>
<td>4.0 to 5.5V</td>
<td>4.0 to 5.5V</td>
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<td>Operating ambient temperature</td>
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<td>–40°C to +85°C, -40°C to +110°C</td>
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### Item 2

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<td>29 MIPS (20 MHz)</td>
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<td>Data bus: –</td>
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<td>Memory controller</td>
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<td>Interrupt sources</td>
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<td>External: 12 (12/16)</td>
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<tr>
<td>Timer/counter</td>
<td>16-bit timer/event counter (TMM) = 4 ch</td>
<td>16-bit timer/event counter (TMM) = 4 ch</td>
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<td>16-bit interval timer (TMM) = 1 ch</td>
<td>16-bit interval timer (TMM) = 1 ch</td>
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<td>CSI = 2 ch</td>
<td>UART (LIN compatible) = 3 ch</td>
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<td>4 ch</td>
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<td>Debug control unit</td>
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<td>Provided (RUN, break)</td>
<td>Provided (RUN, break)</td>
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<td>Other peripheral functions</td>
<td>Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 2 ch</td>
<td>Watch timer: 1 ch, on-chip POC/LVI, RAM hold flag, aFCAN controller: 2 ch</td>
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<td>170 mW (@5.0 V, 20 MHz)</td>
<td>155 mW (@5.0 V, 20 MHz)</td>
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<td>Package</td>
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<td>144-pin LQFP (20 × 20 mm)</td>
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<td>–40°C to +85°C, -40°C to +110°C</td>
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## ASSP Lineup (3/3)

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<th>V850SF1B1</th>
<th>V850SF1BY</th>
<th>V850SF3080</th>
<th>V850SF3080Y</th>
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<td>V850SF1</td>
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<td>16 MOPS (@ 16 MHz) 25 MOPS (@ 32 MHz)</td>
<td>16 MOPS (@ 16 MHz) 25 MOPS (@ 32 MHz)</td>
<td>16 MOPS (@ 16 MHz) 25 MOPS (@ 32 MHz)</td>
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<td>128 KB (mask) 256 KB (flash) 128 KB (mask) 256 KB (flash) 128 KB (mask) 256 KB (flash) 128 KB (mask) 256 KB (flash)</td>
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<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
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<td>SRAM, etc.</td>
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<td>SRAM, etc.</td>
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<td>Watch timer: 1 ch, 12- to 16-bit PWM output: 4 ch, V_sync/H_sync separator, ROM correction function: 4 points</td>
<td>Watch timer: 1 ch, 12- to 16-bit PWM output: 4 ch, V_sync/H_sync separator, ROM correction function: 4 points</td>
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<td>16- to 40.5 MHz</td>
<td>16- to 40.5 MHz</td>
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<td>8-ch (6 inputs)</td>
<td>8-ch (6 inputs)</td>
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<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
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Note 1: Number of external interrupts that can be used to release STOP mode
Note 2: Only Y products have an on-chip I 2 C interface.
### High-End Lineup (1/2)

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<tr>
<th>Item</th>
<th>µPD703131A/3131AY</th>
<th>µPD703132A/3132AY</th>
<th>µPD703133A/3133AY</th>
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<th>µPD70F3134A/F3134AY</th>
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<td>µPD703103A</td>
<td>µPD703105A</td>
<td>µPD703106A</td>
<td>µPD703107A</td>
<td>µPD70F3107A</td>
<td>µPD703108</td>
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#### µPD703103A

- **CPU core**: V850E1
- **CPU performance**: 106 MIPS (@ 80 MHz)
- **Internal ROM**: 256 KB (mask)
- **Internal RAM**: 16 KB
- **External bus interface**: Multiple/optional, separate
- **Memory controller**: SDRAM, SRAM, etc.
- **Interrupt sources**: Internal
- **Port types**: 1 ch
- **Watchdog timer**: C
- **Serial interface**: CSI, UART (1 ch)
- **A/D converter**: 8-bit (x 8 ch)
- **DMA controller**: 4 ch
- **Package**: 144-pin LOFP (20 x 20 mm)
- **Power supply voltage**: 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external)
- **Power consumption (Typ.):** 1.40 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power consumption (Max.):** 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power supply voltage**: 3.0 to 3.6 V
- **Power consumption (Max.):** 3.0 to 3.6 V
- **Power consumption (Max.):** 528 mW (@ 3.3 V, 50 MHz)
- **Temperature**: -40°C to +85°C

#### µPD703105A

- **CPU core**: V850E1
- **CPU performance**: 167 MIPS (@ 80 MHz)
- **Internal ROM**: ROM-less 128 KB (mask) 256 KB (flash)
- **Internal RAM**: 16 KB
- **External bus interface**: Multiple/optional
- **Memory controller**: SDRAM, SRAM, etc.
- **Interrupt sources**: Internal
- **Port types**: 1 ch
- **Watchdog timer**: C
- **Serial interface**: CSI, UART (1 ch)
- **A/D converter**: 8-bit (x 8 ch)
- **DMA controller**: 4 ch
- **Package**: 144-pin LOFP (20 x 20 mm)
- **Power supply voltage**: 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external)
- **Power consumption (Typ.):** 1.40 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power consumption (Max.):** 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power supply voltage**: 3.0 to 3.6 V
- **Power consumption (Max.):** 528 mW (@ 3.3 V, 50 MHz)
- **Temperature**: -40°C to +85°C

#### µPD703106A

- **CPU core**: V850E1
- **CPU performance**: 106 MIPS (@ 80 MHz)
- **Internal ROM**: ROM-less 256 KB (flash)
- **Internal RAM**: 16 KB
- **External bus interface**: Multiple/optional
- **Memory controller**: SDRAM, SRAM, etc.
- **Interrupt sources**: Internal
- **Port types**: 1 ch
- **Watchdog timer**: C
- **Serial interface**: CSI, UART (1 ch)
- **A/D converter**: 8-bit (x 8 ch)
- **DMA controller**: 4 ch
- **Package**: 144-pin LOFP (20 x 20 mm)
- **Power supply voltage**: 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external)
- **Power consumption (Typ.):** 1.40 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power consumption (Max.):** 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power supply voltage**: 3.0 to 3.6 V
- **Power consumption (Max.):** 528 mW (@ 3.3 V, 50 MHz)
- **Temperature**: -40°C to +85°C

#### µPD70F3107A

- **CPU core**: V850E1
- **CPU performance**: 416 MIPS (@ 3.3 V, 40 MHz)
- **Internal ROM**: ROM-less 256 KB (flash)
- **Internal RAM**: 16 KB
- **External bus interface**: Multiple/optional
- **Memory controller**: SDRAM, SRAM, etc.
- **Interrupt sources**: Internal
- **Port types**: 1 ch
- **Watchdog timer**: C
- **Serial interface**: CSI, UART (1 ch)
- **A/D converter**: 8-bit (x 8 ch)
- **DMA controller**: 4 ch
- **Package**: 144-pin LOFP (20 x 20 mm)
- **Power supply voltage**: 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external)
- **Power consumption (Typ.):** 1.40 to 1.65 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power consumption (Max.):** 2.3 to 2.7 V (internal)/3.0 to 3.6 V (external) (@ 150 MHz)
- **Power supply voltage**: 3.0 to 3.6 V
- **Power consumption (Max.):** 416 mW (@ 3.3 V, 40 MHz)
- **Temperature**: -40°C to +85°C
### High-End Lineup (2/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>V850E/MS1</th>
<th>V860E/MS2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Part No.</strong></td>
<td>µPD703100A-33/−40</td>
<td>µPD703100A-33/−40</td>
</tr>
<tr>
<td></td>
<td>µPD703101A-33</td>
<td>µPD703101A-33</td>
</tr>
<tr>
<td></td>
<td>µPD703102A-33</td>
<td>µPD703102A-33</td>
</tr>
<tr>
<td></td>
<td>µPD703102-33</td>
<td>µPD703102-33</td>
</tr>
<tr>
<td></td>
<td>µPD70F3102A-33</td>
<td>µPD70F3102A-33</td>
</tr>
<tr>
<td></td>
<td>µPD70F3102-33</td>
<td>µPD70F3102-33</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850E</td>
<td>V860E</td>
</tr>
<tr>
<td>CPU performance</td>
<td>–</td>
<td>47 MIPS (@ 33 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>96 KB (mask)</td>
<td>128 KB (mask)</td>
</tr>
<tr>
<td></td>
<td>128 KB (flash)</td>
<td>ROM-less</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>4 KB</td>
<td>4 KB</td>
</tr>
<tr>
<td>External bus interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Memory controller</td>
<td>EDO DRAM, SRAM, etc.</td>
<td>EDO DRAM, SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>External</td>
<td>16 (1)</td>
</tr>
<tr>
<td>Time/counter</td>
<td>16-bit timer/event counter = 6 ch</td>
<td>16-bit timer/event counter = 4 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit interval timer = 2 ch</td>
<td>16-bit interval timer = 2 ch</td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Serial interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>A/D converter</td>
<td>16-bit x 8 ch</td>
<td>16-bit x 4 ch</td>
</tr>
<tr>
<td>DMA controller</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
<td>52</td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Other peripheral functions</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>2 to 40 MHz (-40 product)</td>
<td>10 to 33 MHz</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>3.0 to 5.6 V (internal, external) (4 products)</td>
<td>3.0 to 5.6 V (internal/external)</td>
</tr>
<tr>
<td></td>
<td>2 to 3.3 V (33 MHz)</td>
<td>4.5 to 5.5 V (external)</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>2.2 mW (@ 2.2 to 3.3 MHz)</td>
<td>219 mW (@ 2.2 to 3.3 MHz)</td>
</tr>
<tr>
<td></td>
<td>430 mW (@ 5 V, 33 MHz)</td>
<td>515 mW (@ 5 V, 33 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>157-pin FBGA (14 x 14 mm)</td>
<td>100-pin LFQFP (14 x 14 mm)</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

Notes:
1. Number of external interrupts that can be used to release STOP mode
2. µPD703100A-33, 703101A-33, 703102A-33, and 70F3102A-33 only
3. ±1°C to +50°C
4. –40°C to +85°C

---

### V853

<table>
<thead>
<tr>
<th>Item</th>
<th>µPD70003A</th>
<th>µPD70004A</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>µPD703025A</td>
<td>µPD703025A</td>
</tr>
<tr>
<td></td>
<td>µPD70F3025A</td>
<td>µPD70F3025A</td>
</tr>
<tr>
<td>CPU core</td>
<td>V850</td>
<td>V850</td>
</tr>
<tr>
<td>CPU performance</td>
<td>38 MIPS (@ 33 MHz)</td>
<td>38 MIPS (@ 33 MHz)</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>128 KB (mask)</td>
<td>96 KB (mask)</td>
</tr>
<tr>
<td></td>
<td>256 KB (mask)</td>
<td>256 KB (mask)</td>
</tr>
<tr>
<td></td>
<td>128 KB (flash)</td>
<td>256 KB (flash)</td>
</tr>
<tr>
<td>Internal RAM</td>
<td>8 KB</td>
<td>4 KB</td>
</tr>
<tr>
<td>External bus interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Memory controller</td>
<td>SRAM, etc.</td>
<td>SRAM, etc.</td>
</tr>
<tr>
<td>Interrupt sources</td>
<td>Internal</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>External</td>
<td>16 (1)</td>
</tr>
<tr>
<td>Time/counter</td>
<td>16-bit timer/event counter = 4 ch</td>
<td>16-bit timer/event counter = 4 ch</td>
</tr>
<tr>
<td></td>
<td>16-bit interval timer = 1 ch</td>
<td>16-bit interval timer = 1 ch</td>
</tr>
<tr>
<td>Watchdog timer</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Serial interface</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>A/D converter</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>DMA controller</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Ports</td>
<td>I/O</td>
<td>67</td>
</tr>
<tr>
<td>Debug control unit</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Other peripheral functions</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>2 to 33 MHz</td>
<td>2 to 33 MHz</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>4.5 to 5.5V</td>
<td>4.5 to 5.5V</td>
</tr>
<tr>
<td>Power consumption (Typ.)</td>
<td>385 mW (@ 5 V, 33 MHz)</td>
<td>405 mW (@ 5 V, 33 MHz)</td>
</tr>
<tr>
<td></td>
<td>425 mW (@ 5 V, 33 MHz)</td>
<td>480 mW (@ 5 V, 33 MHz)</td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LFQFP (14 x 14 mm)</td>
<td>100-pin LFQFP (14 x 14 mm)</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

Notes:
Number of external interrupts that can be used to release STOP mode
The V850 Series development environment consists of tools designed to make the development of application systems using the V850 Series of high-performance microcontrollers made by NEC Electronics more pleasant, faster, and more accurate. Each one of these development tools features functions to fully exploit the performance of the V850 Series.
Low-Priced Development Environment Lineup

Emulator and evaluation board available at low prices

**Low-priced full-function emulator**

**IECUBE**
- Low prices 1/3 or 1/4 the price of conventional emulators
- Connectable to PC via USB
- Enhanced real-time RAM monitor and time measuring function
- On-chip self-diagnosis function
- Debugger and simple programmer provided
- Palm size

**Ultra-low-priced on-chip emulator**

**N-Wire CARD**
- Ultra low price 1/10 the price of conventional emulators
- Connectable to PC via PCMCIA
- Writing to the microcontroller on-chip flash memory possible
- Debugger provided

**Starter kit for simple evaluation**

**TK-850 Series**
- Evaluation kit enabling easy performance testing
- Lineup for V850ES/Kx1, V850ES/SA2, and V850ES/SG2
- Debugger, compiler, and circuit diagrams provided as standard

* For details, refer to V850 Series Development Environment Pamphlet (U15763E)
Development Tools (1/3)

<table>
<thead>
<tr>
<th>Software tools</th>
<th>Product Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software package</td>
<td>SP850</td>
</tr>
<tr>
<td>C compiler</td>
<td>CA850</td>
</tr>
<tr>
<td>Device file</td>
<td>DF703xxx</td>
</tr>
<tr>
<td>Project Manager</td>
<td>PM plus</td>
</tr>
<tr>
<td>Integrated debugger</td>
<td>ID850</td>
</tr>
<tr>
<td>System simulator</td>
<td>SM850</td>
</tr>
<tr>
<td>Real-time OS</td>
<td>RX850, RX850 Pro</td>
</tr>
<tr>
<td>Task debugger</td>
<td>RD850, RD850 Pro</td>
</tr>
<tr>
<td>System performance analyzer</td>
<td>AZ850</td>
</tr>
<tr>
<td>Middleware</td>
<td>AP703000-Bxxx, AP703100-Bxxx</td>
</tr>
<tr>
<td>Performance analysis tool</td>
<td>TW850</td>
</tr>
</tbody>
</table>

Notes 1. Packaged in SP850
2. Downloaded from the NEC Electronics Website. (URL: http://www.necel.com/micro/index_e.html)
3. Included with CA850
4. Included with IECUBE and IE-V850E1-CD-NW.
5. Instruction simulation version: Included with SP850.
   Instruction + peripheral simulation version: Only the SM plus for the μPD70F3261Y is included with SP850.
6. Included with RX850, RX850 Pro

Remark  For details, refer to the V850 Series Development Environment Pamphlet (U15763E).
### Development Tools (2/3)

#### Hardware tools (when using IECUBE)

<table>
<thead>
<tr>
<th>Target Device</th>
<th>In-Circuit Emulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850ES/S2, V850ES/S2</td>
<td>QB-V850ESX2-ZZ</td>
</tr>
<tr>
<td>V850ES/K1, V850ES/KA1, V850ES/KF, V850ES/KF1, V850ES/KF1+</td>
<td>QB-V850ESK1H-ZZ</td>
</tr>
</tbody>
</table>

Remarks:
1. A separate socket is required for each above emulator.
2. A power supply, a USB interface cable, a debugger, and a simple programmer are included. A PC interface board is not required.
3. For details, refer to the V850 Series Development Environment Pamphlet (U15763E).

#### Hardware tools (when using N-Wire CARD)

<table>
<thead>
<tr>
<th>Target Device</th>
<th>On-Chip Debug Emulator</th>
</tr>
</thead>
</table>

Remarks:
1. A target connection cable, a connector conversion board, a target connector, and a debugger are included.
2. A power supply and a PC interface board are not required.
3. For details, refer to the V850 Series Development Environment Pamphlet (U15763E).

#### Hardware tools (using other emulators)

<table>
<thead>
<tr>
<th>Target Device</th>
<th>Main Unit</th>
<th>In-Circuit Emulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>V850ES/S2A2, V850ES/SA3</td>
<td>IE-V850ES-G1</td>
<td>IE-703204-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/S2F1, V850ES/G1, V850ES/KJ1</td>
<td></td>
<td>IE-703217-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/G2, V850ES/G2F</td>
<td></td>
<td>IE-703288-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/PM1</td>
<td></td>
<td>IE-703228-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/FE2, V850ES/FF2, V850ES/F2G, V850ES/F2G</td>
<td></td>
<td>IE-703239-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/ST2</td>
<td></td>
<td>IE-703220-G1-EM1***</td>
</tr>
<tr>
<td>V850ES/SV2</td>
<td>IE-V850E-MC-A</td>
<td>IE-703166-MC-EM1</td>
</tr>
<tr>
<td>V850ES/MA1, V850ES/MA2</td>
<td>IE-V850E-MC</td>
<td>IE-703107-MC-EM1***</td>
</tr>
<tr>
<td>V850ES/IA1</td>
<td>IE-V850E-MC</td>
<td>IE-703116-MC-EM1</td>
</tr>
<tr>
<td>V850ES/IA2</td>
<td></td>
<td>IE-703114-MC-EM1</td>
</tr>
<tr>
<td>V850ES/MS1 (5V), V850ES/MS2 (5V)</td>
<td></td>
<td>IE-703102-MC-EM1***</td>
</tr>
<tr>
<td>V850ES/MS1 (3.3V)</td>
<td></td>
<td>IE-703102-MC-EM1A</td>
</tr>
<tr>
<td>V850/SA1</td>
<td>IE-703002-MC</td>
<td>IE-703017-MC-EM1***</td>
</tr>
<tr>
<td>V850/SB1, V850/SB2</td>
<td>IE-703002-MC</td>
<td>IE-703037-MC-EM1***</td>
</tr>
<tr>
<td>V850/SV1</td>
<td></td>
<td>IE-703040-MC-EM1***</td>
</tr>
<tr>
<td>V850/SF1</td>
<td></td>
<td>IE-703079-MC-EM1***</td>
</tr>
<tr>
<td>V850/SC1, V850/SC2, V850/SC3</td>
<td></td>
<td>IE-703089-MC-EM1</td>
</tr>
<tr>
<td>V850</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. A separate socket and probe are required for connection to the target system.
2. A separate socket is required for connection to the target system.
3. Depending on the target device package, a separate socket and probe may be required.
   - The optional PC interface board (IE-70090-PCI-F-A or IE-70000-CD-F-A) are required as a common part.
   - Power supply: IE-70000-MC-PS-B

Remark:
For details, refer to the V850 Series Development Environment Pamphlet (U15763E).
In-circuit emulator (IECUBE)
1. In-circuit emulator (IECUBE)
2. AC adapter (provided with ①)
3. USB interface cable (provided with ⑦)
4. Extension probe
5. Exchange adapter (provided with ⑥ Note)
6. Target connector (provided with ① Note)
7. Mount adapter

configuration example

Host machine (with PCMCIA slot)
1. Host machine (with PCMCIA slot)
2. On-chip emulator IE-V850E1-CD-NW
3. In-circuit emulator connection cable
4. Connector conversion board
5. In-circuit emulator connector

IE-V850ES-G1 configuration example

1. In-circuit emulator (main unit)
2. Emulation board (connected inside main unit)
3. Emulation probe
4. Conversion adapter/conversion socket
5. PC interface cable (provided with ⑦)
6. Power supply cable (provided with ⑦)

N-Wire CARD configuration example

1. In-circuit emulator (main unit)
2. Option board
3. Power supply unit
4. Conversion adapter/conversion socket (provided with ②)
5. PC interface cable (provided with ①)

Note: If ordering the in-circuit emulator (①), if the part number ends in “-ZZZ”, the above exchange adapter (⑤) and target connector (⑥) are not provided.
Note: The RD850, RD850 Pro, and AZ850 can be used with the ID850, ID850QB, MULTI, PARTNER, and WATCHPOINT.

ATI: Accelerated Technology, Inc.
CATS: Communication and Technology Systems, Inc.
GAIO: Gaio Technology Co., Ltd.
GHS: Green Hills Software, Inc.
KMC: Kyoto Microcomputer Corporation
Metros werks: Metrowerks Corporation

Midas Lab Co., Ltd.
MSP0, Inc.
Red Hat Corporation
Sophia Systems Co., Ltd.
Yokogawa Digital Computer Corporation
NEC Electronics
Development environment using ROM emulator, evaluation board

V850 Series Development Environment (2/2)

Evaluation board

- Low-cost evaluation board (limited functions)

Real-time OS
Task debugger
Compiler
Debugger
Analyzer
ROM emulator

- Evaluation board

- RD850 Note
- RD850 Pro Note
- RX850
- RX850 Pro
- CA850
- KMC
- exeGCC
- NORTi
- Nucleus PLUS
- ATI
- GHS
- CCV850
- CCV850E
- MULTI
- AZ850
- PARTNER
- KMC
- emgcc
- PARTNER-ET II
- GHS
- XDEB-V
- SystemSimulator
- GAIO
- Native-G
- XCC-V
- XASS-V
- Monitor version DB50

Note: RD850, RD850 Pro, and AZ850 can be used with MULTI, PARTNER.

- APPLY: Application Corporation
- ATI: Accelerated Technology, Inc.
- Cosmo: Cosmo Co., Ltd.
- Red Hat: Red Hat Corporation
- GAIO: Gaio Technology Co., Ltd.
- GHS: Green Hills Software, Inc.
- KMC: Kyoto Microcomputer Corporation
- Lightwell: Lightwell Co., Ltd.
- Metrowerks: Metrowerks Corporation
- Midas Lab: Midas Lab, Co., Ltd.
- Midoriya: Midoriya Electric Co., Ltd.
- Mispo: Mispo, Inc.
- WRS: Wind River Systems, Inc.
- eSOL: eSOL Co., Ltd.
- Unmarked: NEC Electronics

- SG-703107-1
- SG-703111-1
- RTE-V852-PC
- RTE-V853-PC
- RTE-V850E/MA3-PC
- RTE-V850E/IA1-PC
- RTE-V850ES/FJ2-PC
- RTE-V850ES/SJ2-PC
**Software package (SP850)**

**Product configuration**
The SP850 software package consists of the following software development tools.
- C compiler (CA850)
- Project Manager (PM plus)
- Integrated debugger (ID850, ID850NW) (to be packaged)
- System simulator (SM850, SM plus) (to be packaged)
- Performance analysis tuning tool (TW850)
- Device file (DF703xxx)

**Features**
- Complies with ANSI-C, a C language standard.
- Supports libraries for embedded systems
- Compact code size and faster execution speed can be realized through powerful optimization
- Utilities useful for embedded systems (ROMization processor, etc.)
- Description of embedded systems in C language (specification of memory allocation and I/O register access) is possible.

**System simulator (SM850, SM plus)**

**Features**
- Same operability as debugger
- Target-less evaluation prior to target completion possible
- In addition to the operation of the CPU itself, target system operation including on-chip peripheral unit and interrupt servicing can also be simulated.
- Pseudo-target system construction and I/O operation are possible through external parts.
- Data generated by 0/1 logic and timing charts can be input to the program being simulated.
- Larger number of events than in-circuit emulator
- Execution speed estimates can be done on the host machine to accurately simulate pipeline operation
- Construction by user target system users is possible through user open interface
- A peripheral I/O register status can be specified and when this status occurs, the system can be made to output an interrupt at the desired timing or transfer data to memory (peripheral I/O register event & action function).

**Target devices**

**Note**
The pipeline mode is supported by the V853.

**Project manager (PM plus)**

**Features**
- Project management (management of target chip, source, and environment during debugging is possible.)
- Supports wizard function during project creation
- Automation of series of operations consisting of edit, build, and debug
- Integration of Help function

**C compiler (CA850)**

**Features**
- Supports libraries for embedded systems
- Compact code size and faster execution speed can be realized through powerful optimization
- Utilities useful for embedded systems (ROMization processor, etc.)
- Description of embedded systems in C language (specification of memory allocation and I/O register access) is possible.

**Software Product**

**N-Wire card (IE-V850E1-CD-NW)**

**Features**
- Supports V850E and V850ES
- Emulator for on-chip debugging
- Enables realization of low-cost development environment
- Compact PC card type
- Function for download to internal flash ROM
- Same ease of operation as ID850

**Target Devices**
Development Environment

Integrated debugger (ID850, ID850NW, ID850QB)

- **Features**
  - Supports object files
  - Debugging at source level
  - Debugging using target resources
  - Real-time execution on target
  - Event setting according to complex software operation
  - Online help function

Task debuggers (RD850, RD850 Pro)

- **Features**
  - Display detailed information on OS resources such as tasks.
  - Display source of referenced tasks.
  - Included with real-time OS (RX850, RX850 Pro)

Real-time OSs (RX850, RX850 Pro)

- **Features**
  - Comply with global standard (µTRON 3.0 specifications).
  - Support power management function.
  - Enable embedding of required functions only (selection of system calls to be used).
  - Support sophisticated task development through task debugger (RD).
  - Support application operation analysis through system performance analyzer (AZ)
  - Inherit attributes of real-time OS of 16-bit V Series and 78K Series

System performance analyzer (AZ850)

- **Features**
  - Detection of bugs through system timing errors
  - Detection of bugs due to simultaneous operation of complex tasks
  - Detection/analysis of real-time system execution performance
  - Operation linked to various debuggers

TCP/IP software library (RX-NET) for V850E products

- **Features**
  - TCP/IP protocol stack
  - Applications
  - LAN control driver

- **Product configuration**
  - RFC-compliant
  - Support of numerous socket interfaces/libraries
  - Support of applications as option products
  - Provided device driver
  - Support of NEC Electronics real-time OS (RX850 Pro)

Target devices

- V850E products

Performance analysis tuning tool (TW850)

- **Features**
  - Performance analysis changing the internal ROM size, instruction cache size, etc., is possible.
  - Display of inter-function call relationships, call count information, function execution time information, and cache mishit information
  - Functions optimally placed to reduce cache mishit count
  - Functions causing bottlenecks placed into internal ROM or other high-speed access memory

In-circuit emulator (IE, IECUBE)

- **Features**
  - Emulator functions loaded in dedicated chip to realize high equivalence
  - Connectable to variety of computers
  - Large array of emulation functions
  - Realization of maximum operating frequency equivalent to that of device

Performance analysis tuning tool (TW850)
OSEK/VDX specifications compliant OS (RX-OSEK850)

- **Features**
  - **Kernel**
    - Compliant with OSEK/VDX OS Ver. 2.0 specifications
    - Supports 4 conformance classes: BCC1, BCC2, ECC1, and ECC2.
  - **Configurator**
    - Configurator (OIL850) allowing easy system information creation provided as standard.
    - Configuration files support formats compatible with OIL Ver. 2.0.
  - **Task debugger (RD-OSEK850)**
    - Task debugger effective for application debugging using RX-OSEK850 provided as standard

RISC microcontroller reference platform (SolutionGear™)

- **Features**
  - General-purpose evaluation boards available as RISC microcontroller software development platform
  - Target CPU: V850E/MA1, V850E/ME2
  - Industry standard PC-compatible interfaces including PCI, ISA, PCMCIA, E-IDE, Ethernet™, Serial, Parallel, PS/2, and USB, provided
  - CPU independent motherboards and CPU boards used combined
  - Bundled real-time OS, middleware, and sample drivers
  - MULTI-PARTNER remote monitor version can be used
  - Reference design information provided

Cooperation with third parties

By deepening cooperation with third-party companies and forming an array of tools combining NEC Electronics-made tools and third-party-made tools, NEC Electronics offers development environments that support the diverse needs of users.
Information about V850 microcontrollers and V850 microcontroller development environment can be viewed at the NEC Electronics Microcomputer website.

http://www.necel.com/micro/index_e.html

Microcontroller Search Tool
- Facility for searching for V850 Series microcontrollers by function

Product Lineup
- Microcontroller product information

Document Download
- Microcontroller, development environment, and middleware documents can be downloaded from this area.


Development Tool Download
- V850 Series development tools can be downloaded from this area. Customers who are registered users receive upgrade information by email.

Microcontroller Search Tool

Facility for searching V850 Series microcontrollers by function.

Specify search condition(s) here.

The corresponding NEC Electronics development environment documents can be searched from here with a single link.
Product Lineup

NEC ELECTRONICS

32bit V850 Series
Core release of CPU is completed.
In the midst of product development plan

High-End evolution
- Highly efficient pursuit, MEC, On-chip DMA
- Frequency: 33～150MHz
- Memory ROM: 64～660KB
- Size ROM: 4～16KB
- PKG: 100～144-pin (QFP/FBGA)

ASSP evolution
- Inverter control
- DVC control
- Airbag control
- Car audio control
- Electric power meter control
- Car electronics control
- Frequency: 16～64Hz
- Memory: Size ROM: 64～640KB
- RAM: 4～48KB
- PKG: 64～257-pin (QFP/FBGA)

Middle-range evolution
- Realization of a low EMI noise
- Frequency: 20～32MHz
- Memory: Size ROM: 64～660KB
- RAM: 4～48KB
- PKG: 100～144-pin (QFP/FBGA)

Low-end evolution
- Pursuit of performance
- Frequency: 33MHz
- Memory: Size ROM: 64～256KB
- RAM: 4～16KB
- PKG: 64～144-pin (QFP)
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