MC14433

2

3½ DIGIT A/D CONVERTER

The MC14433 is a high-performance, low-power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual-slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range of 1.999 volts or 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-Series CMOS specifications and can drive a low-power Schottky TTL load.

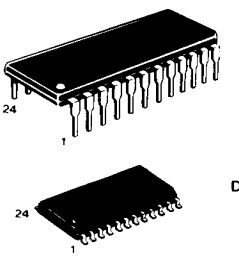
The high-impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, A/D control systems, and in MPU systems.

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions per Second
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs — Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD displays
- Low External Component Count
- Chip Complexity: 1326 FETs

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

3½ DIGIT A/D CONVERTER



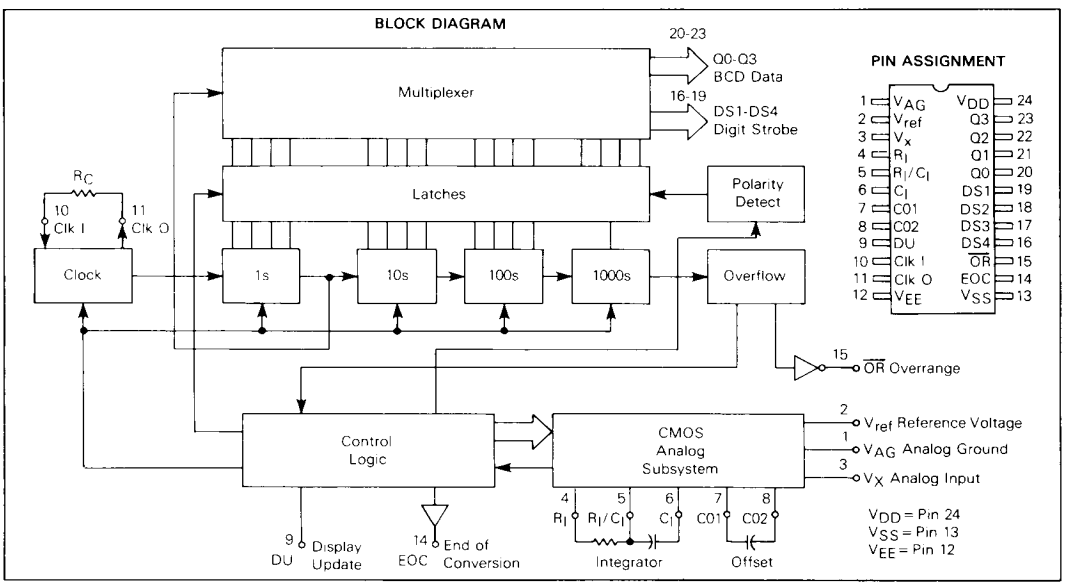
P SUFFIX
PLASTIC DIP
CASE 709

DW SUFFIX
SOG
CASE 751E

ORDERING INFORMATION

MC14433P	Plastic DIP
MC14433DW	SOG Package

BLOCK DIAGRAM



PIN ASSIGNMENT

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	−0.5 to +18	V
Voltage, any pin, referenced to V_{EE}	V	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	−2.8 to −8.0	
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_o	0.1 ± 20%	μF

ELECTRICAL CHARACTERISTICS (C_l = 0.1 μF mylar, R_l = 470 kΩ@V_{ref} = 2.000 V, R_l = 27 kΩ@V_{ref} = 200.0 mV, C_o = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1, unless otherwise indicated)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ#	25°C Max	85°C Min	85°C Max	Unit
Linearity-Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	−5.0	–	–	−0.05 −1 Count	±0.05	+0.05 +1 Count	–	–	
(V_{ref} = 200.0 mV)		5.0	−5.0	–	–	–	±0.05	–	–	–	
Stability — Output Reading											
(V_X = 199.0 mV, V_{ref} = 200.0 mV)	–	5.0	−5.0					3			LSD
Symmetry — Output Reading (Note 2)											
(V_{ref} = 2.000 V)	–	5.0	−5.0					4			LSD
Zero-Output Reading											
(V_X = 0 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0	0	–	–	LSD
Bias Current — Analog Input	–	5.0	−5.0	–	–	–	±20	±100	–	–	pA
Reference Input		5.0	−5.0	–	–	–	±20	±100	–	–	
Analog Ground		5.0	−5.0	–	–	–	±20	±500	–	–	
Common Mode Rejection (f_{clk} = 32 kHz,											
V_X = 1.4 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	65	–	–	–	dB
Input Voltage* Pins 9, 10 "0" Level	V_{IL}										V
(V_O = 4.5 or 0.5 V)		5.0	–	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}										V
(V_O = 0.5 or 4.5 V)		5.0	–	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	–	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	–	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage — Pins 14 to 23											V
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	−5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	5.0	–	4.95	–	
(V_{SS} = −5.0 V) "0" Level	V_{OL}	5.0	−5.0	–	−4.95	–	−5.0	−4.95	–	−4.95	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current — Pins 14 to 23											mA
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	−5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	−5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = −5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	−5.0	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OL} = −4.5 V) Sink	I_{OL}	5.0	−5.0	1.6	–	1.3	2.25	–	0.9	–	
Input Current — DU, Pin 9	I_{DU}	5.0	−5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Quiescent Current	I_Q	5.0	−5.0	–	3.7	–	0.9	2.0	–	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	−8.0	–	7.4	–	1.8	4.0	–	3.2	
DC Supply Rejection											
(V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0.5	–	–	–	mV/V

Notes: 1. Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

2. Symmetry — Defined as the difference between a negative and positive reading of the same voltage at or near full scale.

*Referenced to V_{SS} for Pin 9. Referenced to V_{EE} for Pin 10.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

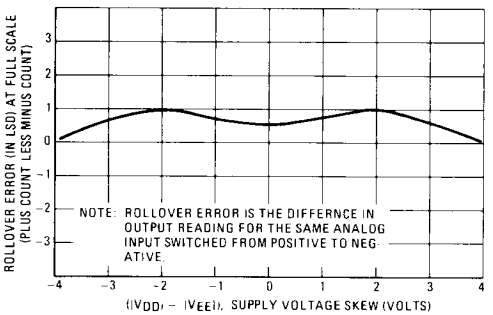


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

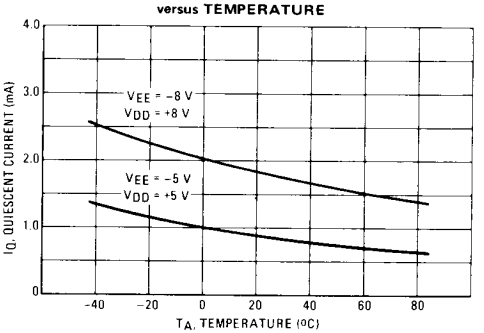


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT AT VDD–VSS = 5 VOLTS

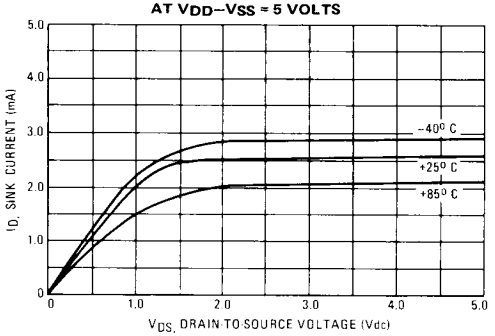


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT AT VDD–VSS = 5 VOLTS

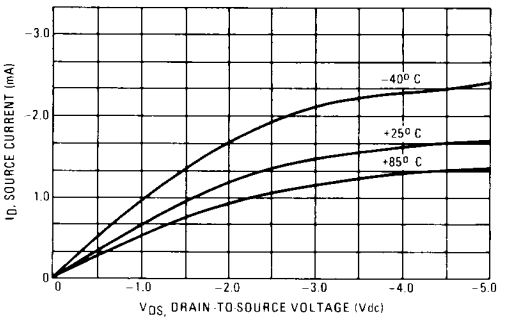


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

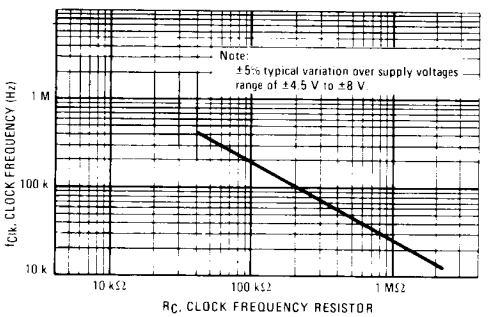
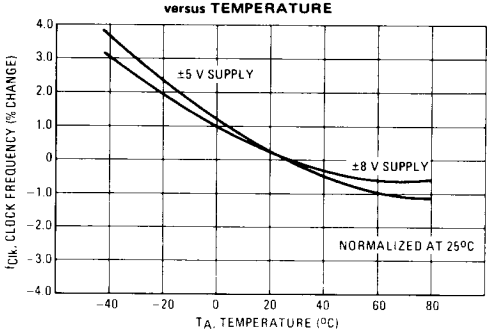


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

2

PIN DESCRIPTIONS

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input. The allowable operating range for V_{AG} is from V_{EE} +2.8 V to V_{DD} −4.5 V.

REFERENCE VOLTAGE (V_{ref}, Pin 2)
UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, Pin 2 functions as a reset for the A/D converter. When Pin 2 is switched low (referenced to V_{EE}) for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (polystyrene or mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T}{\triangle V}$$

$$\triangle V = V_{DD} - V_X(max) - 0.5\ V$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:

R_I is in kΩ
V_{DD} is the voltage at Pin 24 referenced to V_{AG}
V_X is the voltage at Pin 3 referenced to V_{AG}, in V
f_{Clk} is the clock frequency at Pin 10 in kHz
C_I is in μF, △V is in Volts
T is the conversion time, in ms

Example:

$C_I = 0.1\ \mu F$
$V_{DD} = 5.0$ volts
$f_{Clk} = 66$ kHz
For $V_X(max) = 2.0$ volts
$R_I = 480$ kΩ (use 470 kΩ ± 5%)
For $V_X(max) = 200$ mV
$R_I = 28$ kΩ (use 27 kΩ ± 5%)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow $\triangle V + V_X$ to exceed V_{DD}. The 0.5 V factor in the above equation for △V is for safety margin.

OFFSET CAPACITOR (C01, C02; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF (polystyrene or mylar).

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (Pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, Pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through Pin 13. V_X-V_{EE} should be greater than 0.8 V.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY AND INPUT DU (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$) and the DU input. When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between V_{DD} −3.0 volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a positive pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (Pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select outputs and the EOC signal is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin. $V_{DD} - V_X$ should be greater than 2.5 V. $V_{DD} - V_{EE}$ should be greater than 7.8 V. V_{DD} determines V_{OH} for the digital outputs, and V_{IH} for the digital inputs.

TRUTH TABLE (DS1 = 1)

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table:

Q3 – ½ digit, low for "1", high for "0"

Q2 – Polarity: "1" = positive, "0" = negative

Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

FIGURE 7 – ALTERNATE OSCILLATOR CIRCUITS

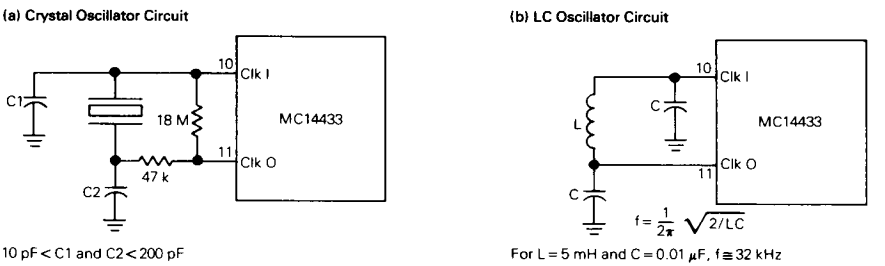


FIGURE 8 – DIGIT SELECT TIMING DIAGRAM

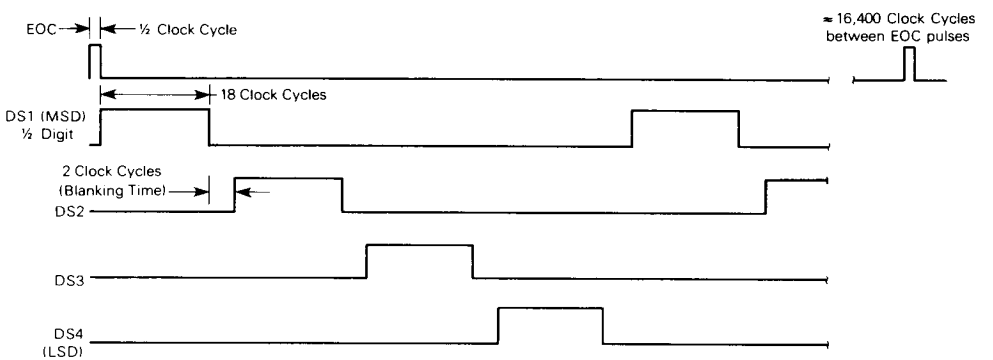


FIGURE 9 — INTEGRATOR WAVEFORMS AT PIN 6

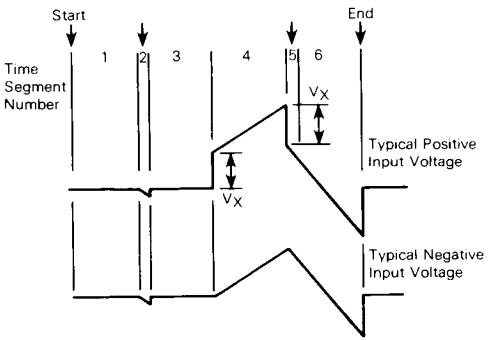
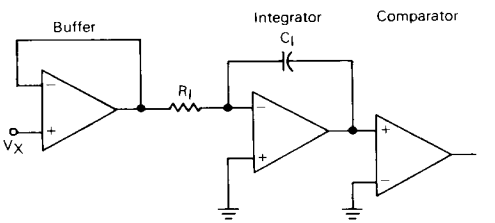


FIGURE 10 — EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 — The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

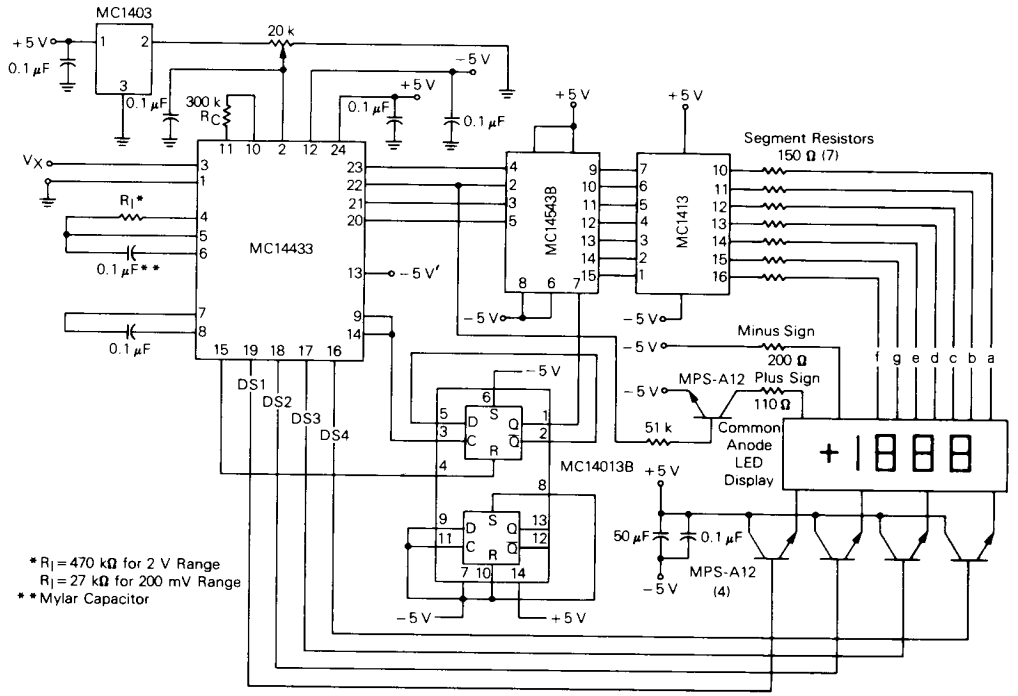
Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input of the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433 for a negative input voltage. When a positive input voltage is applied the buffer input is grounded and V_X is applied to the positive terminal which causes the integrator output to instantaneously jump by the magnitude of V_X as shown in the top waveform in Figure 9. This segment is exactly 4000 clock periods.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 cycle periods. A BCD counter is reset to 0 at the beginning of Segment 6 and then begins to count up. When the output of the integrator causes the comparator to change state the BCD counter value is strobed into output latches to be multiplexed to the displays. The BCD counter continues to count, however, until it rolls over from 1999 to 0000. At this point the sequence counter is clocked back to sequence 1 and an end of conversion pulse is generated.

FIGURE 11 — 3½ DIGIT VOLTMETER—COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

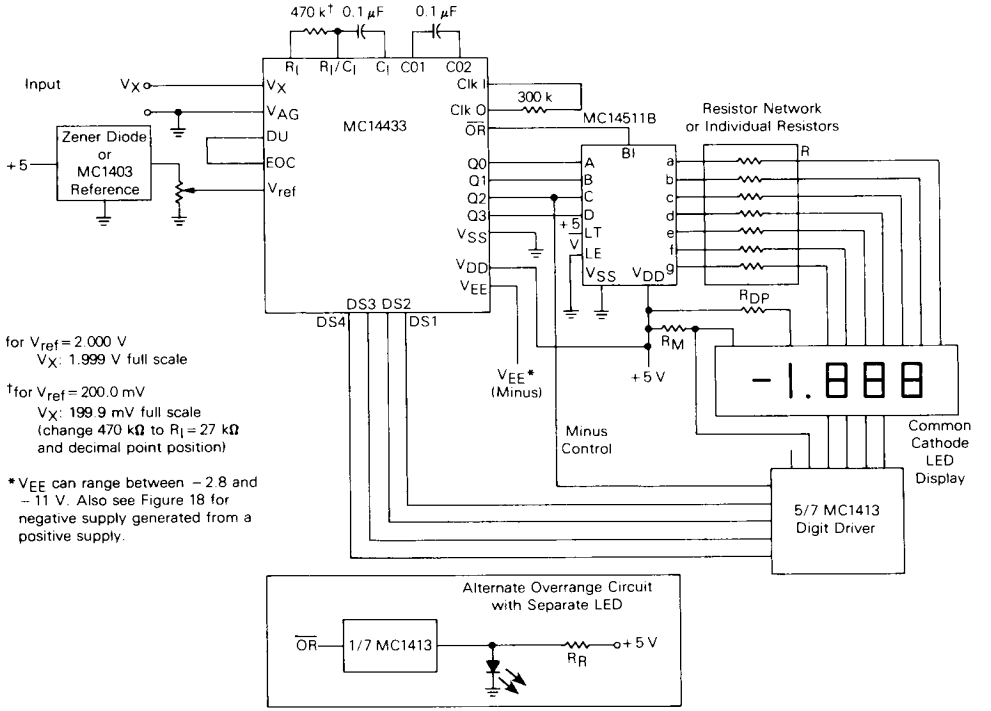
When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and −5 V supplies is *not* required. See the recommended operating conditions and Figure 1.

2

FIGURE 12 — 3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT



3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC1413 provides sink for digit current. (The MC1413 is a device with 7 Darlingtons with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP}. Since the brightness and the type and size of LED display are the choice of the designer, the values of resistors R, R_M, R_{DP}, and R_R that govern brightness are not given.

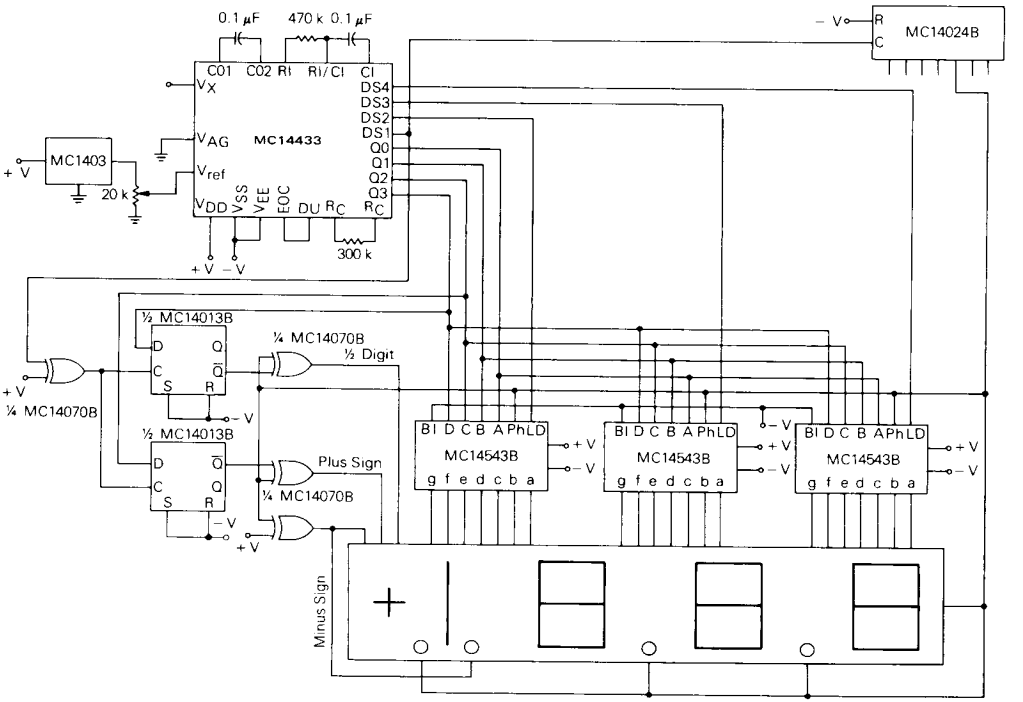
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of the LCD and to the individual segments through the combination of the output cir-

FIGURE 13 — 3½ DIGIT VOLTMETER WITH LCD DISPLAY



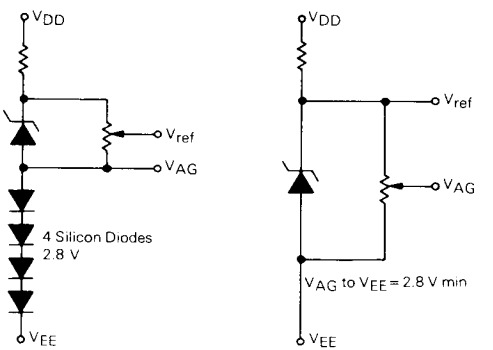
cuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE}. In this case a level must be set for analog ground, V_{AG}, which must be at least 2.8 V above V_{EE}. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE}, leaving 6 V for V_{DD} to V_{AG}. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 — TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY



2

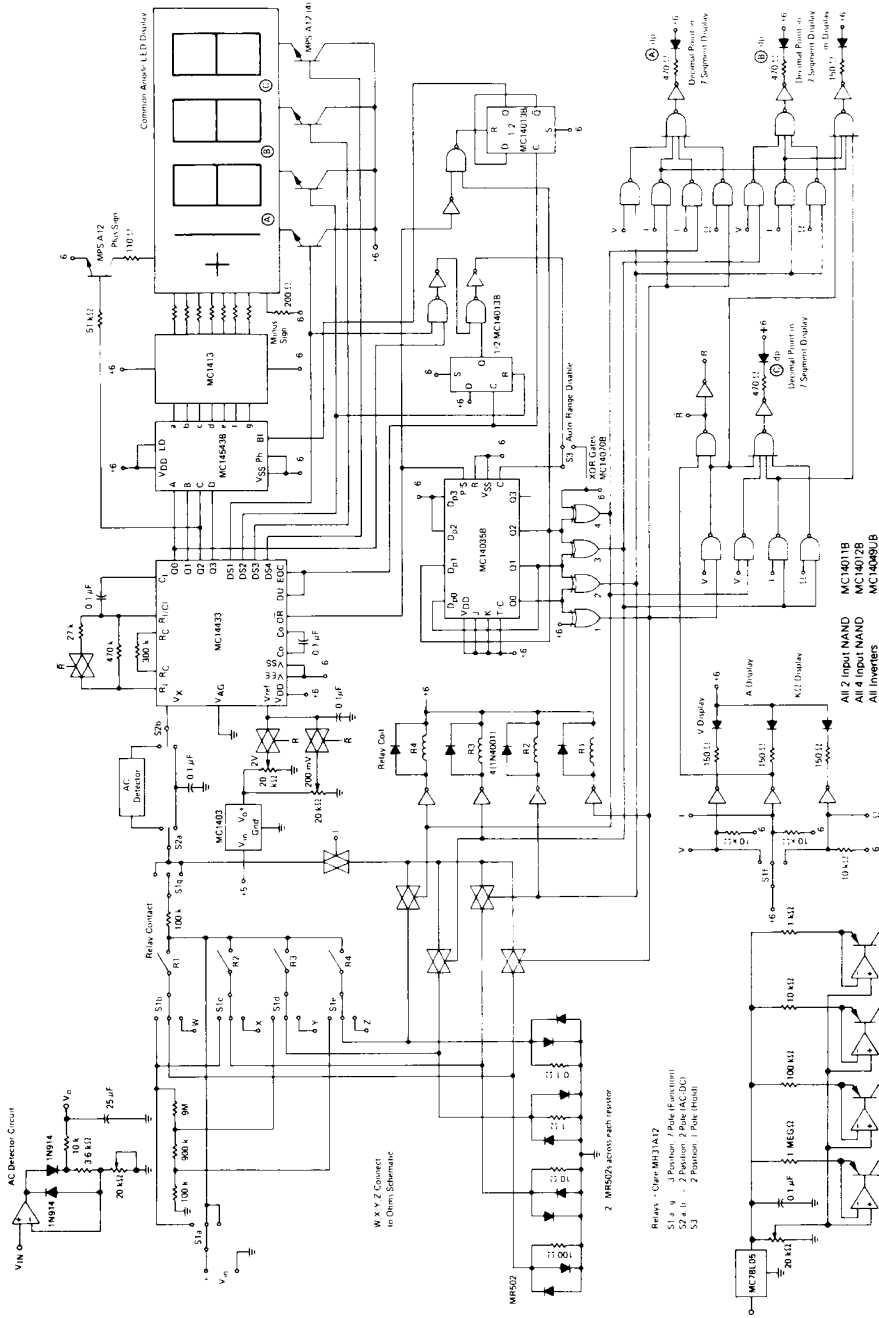


FIGURE 15 – 3½ DIGIT AUTORANGING MULTIMETER

3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 kΩ to 2 MΩ fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

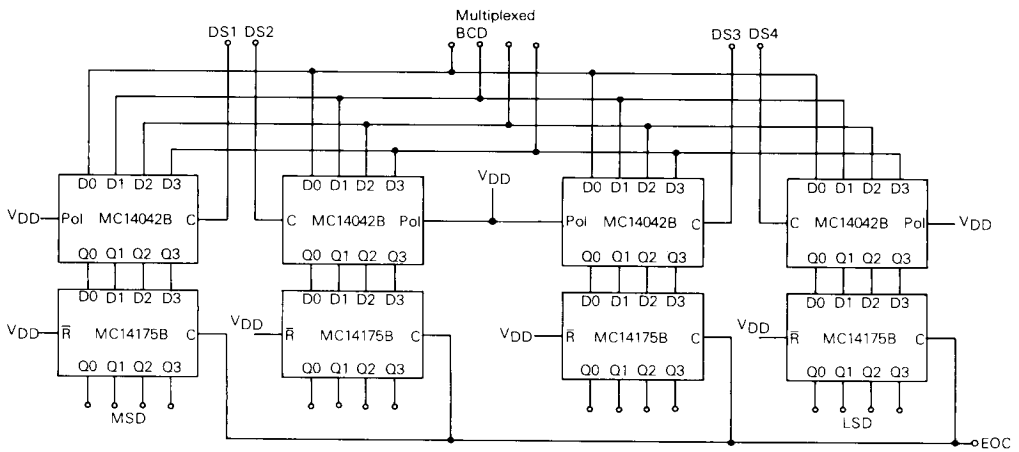
The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits.

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

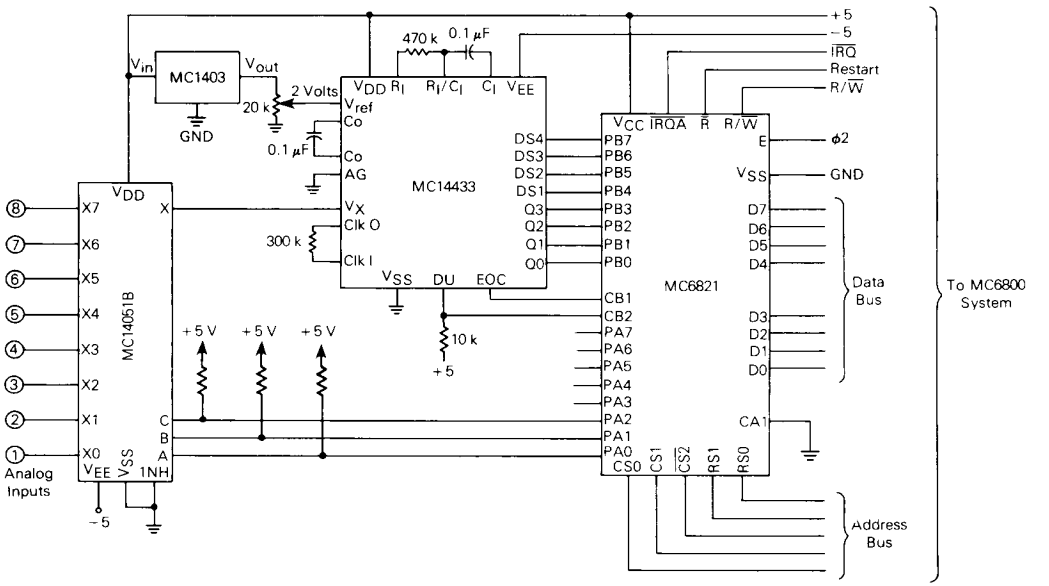
In this system the output ground level is V_{SS}. In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 — DEMULTIPLEXING FOR MC14433 BCD DATA



2

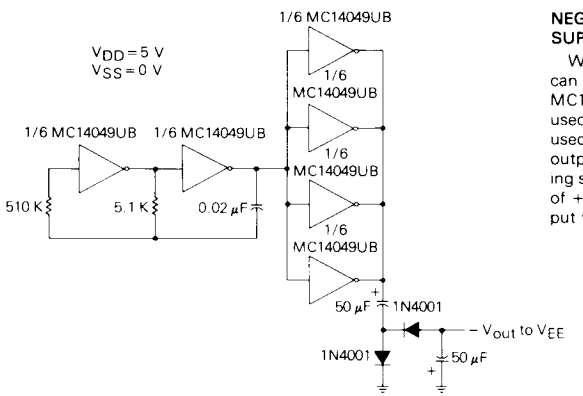
FIGURE 17 – CHANNEL DATA ACQUISITION HARDWARE



8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8-channel data acquisition network using the MC14433 and an MC6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6821 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

FIGURE 18 – NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049UB. Two inverters from CMOS hex inverter are used as an oscillator (≈3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a –4.3 V no load output voltage while the output with a 2 mA load is ≈3.4 V.